HINDUSTAN UNIVERSITY
HINDUSTAN INSTITUTE OF TECHNOLOGY & SCIENCE

# DEPARTMENT OF ELECTRONICS AND COMMUNICATION ENGINEERING

## M.Tech (VLSI Design& Embedded System)

## Out Come based Curriculum and Syllabi
## Regulations 2014-15

*(Applicable to the students admitted from the Academic year 2014- 2015 onwards)*

**Semester I**

| Sl. No | Course Code | Course Title | L | T | P | C | TCH |
|---|---|---|---|---|---|---|---|
| **Theory** | | | | | | | |
| 1. | PMA106 | Advanced Applied Mathematics * | 3 | 1 | 0 | 4 | 4 |
| 2. | PES101 | Digital Signal Processing* | 3 | 1 | 0 | 4 | 4 |
| 3. | PCS105 | Material Science and Engineering* | 3 | 1 | 0 | 4 | 4 |
| 4. | PVL102 | Digital CMOS Design * | 3 | 1 | 0 | 4 | 4 |
| 5. | PCS106 | Solid State Devices* | 3 | 1 | 0 | 4 | 4 |
| 6. | PCS102 | Advanced Radiation Systems* | 3 | 1 | 0 | 4 | 4 |
| **Total** | | | | | | **24** | **24** |

*** Common to CS, PO**

**Semester II**

| Sl. No | Course Code | Course Title | L | T | P | C | TCH |
|---|---|---|---|---|---|---|---|
| **Theory** | | | | | | | |
| 1. | PES102 | Embedded System Design | 3 | 1 | 0 | 4 | 4 |
| 2. | PES104 | Real Time Operating System | 3 | 1 | 0 | 4 | 4 |
| 3. | PVL203 | Digital Signal Processing Structures for VLSI | 3 | 1 | 0 | 4 | 4 |
| 4. | PVL204 | Testing of VLSI Circuits | 3 | 1 | 0 | 4 | 4 |
| 5. | | Elective I | 3 | 0 | 0 | 3 | 3 |
| 6. | | Elective II | 3 | 0 | 0 | 3 | 3 |
| **Practical** | | | | | | | |
| 7. | PVE205 | VLSI Design and Embedded Systems Lab | 0 | 0 | 3 | 2 | 3 |
| **Total** | | | | | | **24** | **25** |

**Semester III**

| Sl. No | Course Code | Course Title | L | T | P | C | TCH |
|---|---|---|---|---|---|---|---|
| **Theory** | | | | | | | |
| 1. | | Elective III | 3 | 0 | 0 | 3 | 3 |
| 2. | | Elective IV | 3 | 0 | 0 | 3 | 3 |
| 3. | | Elective V | 3 | 0 | 0 | 3 | 3 |
| **Practical** | | | | | | | |
| 4. | PVE301 | Project Work (Phase I ) | 0 | 0 | 12 | 6 | 12 |
| **Total** | | | | | | **15** | **21** |

**Semester IV**

| Sl. No | Course Code | Course Title | L | T | P | C | TCH |
|---|---|---|---|---|---|---|---|
| **Practical** | | | | | | | |
| 1. | PVE401 | Project Work (Phase II) | 0 | 0 | 24 | 12 | 24 |
| **Total** | | | | | | **12** | **24** |

**TOTAL CREDITS: 75**

## LIST OF ELECTIVES

| S.No | Course Code | Course Title | L | T | P | C | T C H |
|---|---|---|---|---|---|---|---|
| 1 | PVL201 | ANALOG VLSI DESIGN | 3 | 0 | 0 | 3 | 3 |
| 2 | PVL103 | DIGITAL SYSTEM DESIGN WITH PROGRAMMABLE LOGIC | 3 | 0 | 0 | 3 | 3 |
| 3 | PVL701 | VLSI TECHNOLOGY | 3 | 0 | 0 | 3 | 3 |
| 4 | PVL703 | LOW POWER VLSI DESIGN | 3 | 0 | 0 | 3 | 3 |
| 5 | PVL705 | PHYSICAL DESIGN OF VLSI CIRCUITS | 3 | 0 | 0 | 3 | 3 |
| 6 | PES103 | ADVANCED MICROPROCESSOR | 3 | 0 | 0 | 3 | 3 |
| 7 | PES202 | SOFTWARE TECHNOLOGY FOR EMBEDDED SYSTEMS | 3 | 0 | 0 | 3 | 3 |
| 8 | PES705 | EMBEDDED NETWORKING | 3 | 0 | 0 | 3 | 3 |
| 9 | PES204 | EMBEDDED CONTROL SYSTEMS | 3 | 0 | 0 | 3 | 3 |
| 10 | PCE720 | ADVANCED COMPUTER ARCHITECTURE | 3 | 0 | 0 | 3 | 3 |
| 11 | PCS712 | COGNITIVE RADIO | 3 | 0 | 0 | 3 | 3 |

**SEMESTER-I**
**ADVANCED APPLIED MATHEMATICS**

| L | T | P | C |
|---|---|---|---|
| 3 | 1 | 0 | 4 |

| **PMA106** | **ADVANCED APPLIED MATHEMATICS** | **4 CREDITS** |
|---|---|---|
| **Goal** | Develop the Mathematical skills to formulate certain practical problems, solve them and physically interpret the results | |

| **Objectives** | **Outcomes** |
|---|---|
| The course should enable the student to<br>1. Understand the techniques to solve the system of equations using direct method and indirect methods. Learns to decompose the matrix in the LU form and to find the Eigen value of a matrix using power and Jacobi methods.<br>2. Learn to classify the initial and boundary value problems. Understands the D'Alemberts solution of the one dimensional wave equation. Learn significance of characteristic curves.<br>3. Learn series solutions of Bessel's and Legendre equations. Understand recurrence relation, generating functions and orthogonal properties.<br>4. Learn basics of probability, addition and multiplication, Baye's theorems. Understands the concept of random variable, moment generating function and their properties. Learn standard distributions in discrete and continuous cases<br>5. Learns the different Markovian models with finite and infinite capacity and understands to classify them. | The students should be able to:<br>1. Able to write the algorithm for solving the simultaneous equations for direct and indirect methods. Identifies the Eigen values using conventional method and compares with numerical solutions. Able to write the algorithm to find the Eigen values of a matrix.<br>2. Able to form the wave equations with initial conditions and solve them using D'Alemberts solutions. Solves the wave equations using Laplace transform for displacements in long string – long string under its weight and free and forced vibrations.<br>3. Solves the Bessel's equation and Legendre equations. Using Bessel's function solves many practical problems that arise in electrical transmission problems and vibration of membranes as in loudspeakers.<br>4. Evaluates the probability using addition and multiplication theorem. Applies Baye's for practical problems to find the probability. Verifies whether a given function is a probability mass or density function. Applies the discrete and continuous distributions for solving practical problems. Evaluates the moments of the distributions using moment generating function.<br>5. Able to analyze and classify the models, M / M / 1, M / M / C, finite and infinite capacity and solves practical problems related to the queuing models. |

**UNIT I LINEAR ALGEBRAIC EQUATION AND EIGEN VALUE PROBLEMS 9**

System of Equations – Solution by Gauss Elimination and Gauss Jordan methods – LU decomposition method – Indirect methods – Gauss Jacobi and Gauss Seidel methods – Eigen values of a matrix using Jacobi and power methods.

**UNIT II WAVE EQUATION 9**

Solution of initial and boundary value problems - Characteristics - D'Alembert's solution - Significance of characteristic curves - Laplace transform solutions for displacement in a long string, in a long string under its weight - a bar with prescribed force on one end - Free vibrations of a string.

**UNIT III SPECIAL FUNCTIONS 9**

Series solutions - Bessel's equation - Bessel functions - Legendre's equation - Legendre polynomials - Rodrigue's formula - Recurrence relations - Generating functions and orthogonal property for Bessel functions of the first kind - Legendre polynomials.

**UNIT IVPROBABILITY AND RANDOM VARIABLE 9**

Discrete and Continuous random variables – Moments – Moment generating functions - Standard distributions - Binomial, Poisson, Geometric, Negative Binomial, Uniform, Normal ,Exponential, Gamma and Weibull distributions – Two dimensional random variables – Joint, Marginal and Conditional distributions. Correlation and Regression.

**UNIT VQUEUING THEORY 9**

Markovian models – Birth and death queuing models – Steady state – Single and Multiple servers – M/M/1 – Finite and infinite capacity – M/M/C – finite and infinite capacity.

**L = 45, T=15,TOTAL=60**

**REFERENCES:**


1) Taha, H.A., "Operations Research - An Introduction ", Prentice Hall of India Ltd., 6th Edition, New Delhi, 1997.
2) Dr.Singaravelu A., Dr.Siva Subramanian S., and Dr.Ramachandran C., "Probability and Queuing Theory", Meenakshi agency, 20th edition, January 2013.
3) Veerarajan T., "Probability, Statistics and Random Processes", Tata McGraw-Hill, second edition, 2004.
4) Grewal B.S., "Higher Engineering Mathematics", Khanna Publishers, 34th edition.
5) Sankara Rao K., "Introduction to Partial Differential Equations", PHI, 1995.
6) Veerarajan T., "Mathematics IV", Tata McGraw-Hill, 2000.

## DIGITAL SIGNAL PROCESSING

**L T P C**
**3 1 0 4**

| **PES101** | **DIGITAL SIGNAL PROCESSING** | **4 CREDITS** |
|---|---|---|
| Prerequisite | | |
| Goal | To introduce the Fundamental Concepts of different signal processing techniques using Digital Processors and various transforms and their utility in control systems. | |
| **Objectives** | **Outcomes** | |
| The course should enable the students to :<br><br>(1) Study the Concept of Signals and Systems and their processing techniques.<br><br>(2) Study the Sampling and Quantization techniques and to change the rate of sampling.<br><br>(3) Study the Characteristics and various transform analysis of LTI systems<br><br>(4) Study the design techniques of IIR and FIR filters.<br><br>(5) Study the fundamental concepts of real time Digital Signal Processors. | At the end of the course the student should be able to:<br><br>(1) Understand the various types of Signals and Systems along with their properties.<br><br>(2) Understand the sampling and Reconstruction of Band limited and Band pass signals along-with sampling rate conversion procedures.<br><br>(3) Understand the performance parameters of LTI system and various Transform techniques in Frequency domain.<br><br>(4) Understand the structure and design techniques of IIR and FIR filters and their conversion between domains.<br><br>(5) Know the various type of processors and programming concepts. | |

**UNIT I DISCRETE TIME SIGNALS AND SYSTEMS 9**

Discrete time signal- Basic definition- Some elementary Discrete Time Signals-Representation of signals-Discrete time systems- Basic operation sequences-linear systems-Time invariant systems-Causal systems-Stable systems- Linear time invariant systems-Properties of LTI systems- Linear Constant Coefficient Difference Equations-Fourier Transform Of Discrete Time Signals - Z-Transform-Inverse Z-Transform

**UNIT II SAMPLING OF CONTINUOUS TIME SIGNALS 9**

Periodic Sampling-Reconstruction of Band Limited Signal from its samples- Sampling of Band Pass signals-Sampling rate conversion-Decimation by decimation factors- Inter polarization by an integer Factor-Sampling rate conversion by rational Factor-Sampling rate conversion of Band pass signals-A/D Conversion- Quantization -Coding-D/A conversion.

**UNIT III TRANSFORM ANALYSIS OF LTI SYSTEMS 9**

Ideal filter characteristics-System function and frequency response of LTI systems-Stability and Causality-All pass systems-Minimum phase systems-Discrete Fourier Transform-Relationship between DFT and Fourier Transform of a Discrete Time Signal-Frequency analysis of signals using DFT-Fast Fourier Transform.

**UNIT IV DESIGN OF FILTERS 9**

Block Diagram and signal flow graph representation- Basic structure of IIR Systems-Basic Structure of FIR Systems-Design of FIR Filters -Design of FIR filter by windowing-Classical continuous -Time Low Pass Filter Approximations-Conversion of transfer functions from continuous to discrete Time frequency Transformations of Low Pass Filters.

**UNIT V PRACTICAL DIGITAL SIGNAL PROCESSORS 9**

Fundamentals of Fixed Point DSP architecture-Fixed Point representation of numbers-
Arithmetic computation- Memory accessing-Pipelining of instructions-Features of example processors- Floating point DSPs-Floating point Representation of numbers- Comparison of DSPs.

**L = 45, T=15,TOTAL=60**

**TEXT BOOKS:**

1. Oppenheim and RW Scaffer- Digital Signal Processing-PHI,2000
2. Proakis And Manolakis “Digital Signal Processing: principles, Algorithms and applications “PHI,1992

**REFERENCE:**

1. Rabiner and Gold-Theory and Application of Digital Processing-PHI,1975.

## MATERIAL SCIENCE AND ENGINEERING

**L T P C**

**3 1 0 4**

| **PCS105** | **MATERIAL SCIENCE AND ENGINEERING** | **4 CREDITS** |
|---|---|---|
| **Prerequisite** | - | |
| **Goal** | | |
| **Objectives** | **Outcomes** | |
| The course should enable the students to<br><br>1. Students get the knowledge of Engineering Materials, Basic Structure, Properties and Performance also, about bonding structures<br>**2.** Students are exposed to detailed study on cubic and non-cubic structures Polymorphism, Unit Cell Geometry, Crystal Directions, Planes, Diffraction, Also exposure to Imperfection in crystalline Materials, Order and Disorder in Polymers, Solid Solutions, in Ceramic and Metallic Compounds and Polymers.<br>3. Exposure to **Conductivity and E**nergy Bands, Intrinsic & Extrinsic Semiconductors, and exposure to magnetic materials properties, domain, ceramic magnets, metallic magnets and dia magnetism<br>4. Students study in detail about dielectric and optical ceramics and polymer.<br>5. Exposure is given about Material Service Performance, Corrosion and Control, Effect of Temperatures and radiation | At the end of the course the student should be able to:<br><br>1. Differentiate the materials based on structure, properties and performance and bonding.<br>2. Awareness about cubic and non-cubic Polymorphism, Disorder in Metallic Structures, Polymers and Solutions<br>3. Capable of analyzing depth of conduction in materials about magnetics<br>4. Knowledge about optical properties of dielectric materials, polarization, and about the optical properties of ceramic dielectric transparent materials, Light Emitting Solids.<br>5. Students gain the knowledge about engineering materials under various conditions, effect of corrosion and control. | |

**Unit :1**

**Introduction to Material Science and Engineering**

Materials and Civilization, Materials and Engineering, Structure, Properties and Performance, Types of Materials

**Atomic Bonding and Co-ordination**

Atoms, Ions, Molecules, Macromolecules (Polymers), Three-dimensional bonding, Interatomic distances, Generalizations based on Atomic Bonding.

**Unit :2**

**Crystals**

Cubic & Non-Cubic Structures, Polymorphism, Unit Cell Geometry, Crystal Directions, Crystal Planes, X-Ray Diffraction.

**Disorder in Solid Phase**

Imperfection, Non-crystalline Materials, Order and Disorder in Polymers, Solid Solutions, Solid Solutions in Ceramic and Metallic Compounds, Solid Solutions in Polymers.

**Unit :3**

**Conduction Materials**

Charge Carriers Metallic Conductivity Energy Bands, Intrinsic & Extrinsic Semiconductors, Semiconductor Processing.

**Magnetic Properties of Ceramics and Metals**

Magnetic Materials, Magnetic Domains Ceramic Magnets, Metallic Magnets, Dia Magnetism.

**Unit :4**

**Dielectric and Optical Properties of Ceramics and Polymers**

Dielectric Materials, Polarization Polymeric Dielectrics, Transparent Materials, Light Emitting Solids.

**Unit : 5**

**Performance of Materials in Service**

Service Performance, Corrosion, Corrosion Control, Performance at High Temperatures, Performance of Polymers. Performance of Ceramics at High Temperature, Radiation Damage

**Text :**

1. Lawrence H.Van Vlack Elements of Materials Science and Engineering, Addison – Wesley Publishing Company (Latest Edition)

**References:**

1. B.D. Cullity, Introduction to Magnetic Material's, Addison Wesley Publishing Company
2. M.I.T. Press, Cambridge, Encyclopedia of Materials Science and Engineering
3. L.H.Vanvleck, Materials for Engineers Concepts & Applications
4. OH. Wyahand D.Dew-Hugnes, Metals, Ceramics & Polymers Cambridge, Unit Press.

## DIGITAL CMOS DESIGN

**L T P C**
**3 1 0 4**

| **PVL102** | **DIGITAL CMOS DESIGN** | **4 CREDITS** |
|---|---|---|
| **Prerequisite** | - | |
| **Goal** | The student will get to know the CMOS process technology, CMOS Transistor theory and design of combinational and sequential circuits using CMOS and the basics of verilog programming language. | |
| **Objectives** | **Outcomes** | |
| The course should enable the students to<br><br>6. Study the concept of CMOS transistor theory and CMOS process technology<br><br>7. Study the concept of CMOS inverter and the design of combinational logic circuits ,<br><br>8. Study the concept of sequential circuits with timing issues, clocking strategies and pipeline techniques,<br><br>9. Study the concept of arithmetic building blocks,<br><br>10. Study the concept of Verilog HDL language. | At the end of the course the student should be able to:<br><br>6. Understand the concept of CMOS transistor theory and CMOS process technology,<br><br>7. Understand the concept of CMOS inverter and able to draw stick diagram for the logic gates and design of combinational logic circuits,<br><br>8. Understand the concept of sequential circuits with timing issues, clocking strategies and pipeline techniques,<br><br>9. Understand the concept of arithmetic blocks and also able to design the arithmetic blocks,<br><br>10. Understand the concept of verilog HDL language and able to write verilog code. | |

**UNIT I MOS TRANSISTOR THEORY AND PROCESS TECHNOLOGY 9**

NMOS and PMOS transistors, Threshold voltage –Body effect- Design equations – Second order effects, MOS models and small signal AC characteristics-Basic CMOS technology

**UNIT II CMOS INVERTER AND COMBINATIONAL LOGIC 9**

NMOS and CMOS inverters, Stick diagram, Propagation delay, Examples of combinational logic design, Pass transistor logic – Power dissipation

**UNIT III SEQUENTIAL LOGIC CIRCUITS 9**

Static and Dynamic Latches and Registers, Timing Issues, Pipelines, Clocking strategies, Synchronous and Asynchronous Design.

**UNIT IV DESIGNING ARITHMETIC BUILDING BLOCKS 9**

Datapath circuits, Architectures for Adders, Accumulators, Multipliers, Barrel Shifters, Memory Architectures, and Memory control circuits

**UNIT VVERILOG HARDWARE DESCRIPTION LANGUAGE 9**

Overview of digital design with Verilog HDL, Hierarchical modeling concepts, Modules and port definitions, Gate level modeling, Data flow modeling, Behavioral modeling, Task & functions, Test Bench.

**L = 45, T=15,TOTAL=60**

**REFERENCES:**


1. Jan Rabaey, Anantha Chandrakasan, B Nikolic, “Digital Integrated Circuits: A Design Perspective”. Second Edition, Feb 2003, Prentice Hall of India.
2. N.Weste, K. Eshraghian, “ Principles of CMOS VLSI Design”. Second Edition, 1993 Addision Wesley,
3. M J Smith, “Application Specific Integrated Circuits”, Addisson Wesley, 1997
4. Samir Palnitkar, “Verilog HDL”, Pearson Education, 2nd Edition, 2004.
5. Eugene D.Fabricius, “Introduction to VLSI Design”, McGraw Hill International Editions, 1990.
6. Pucknell, “Basic VLSI Design”, Prentice Hall of India Publication, 1995.

## SOLID STATE DEVICES

**L T P C**
**3 1 0 4**

| **PCS106** | **SOLID STATE DEVICES** | **4 CREDITS** |
|---|---|---|
| **Goal** | The aim of this course is to familiarize the student with the principle of operation, capabilities and limitation of various electron devices so that he will be able to use these devices effectively. | |

| **Objectives** | **Outcomes** |
|---|---|
| The course should enable the student to<br>1. Learn about motion of charge in electric and microtic field effect of force and moving charge calculation of cyclotron frequency, electro static magnetic deflection sensitivity, Fermi - Dirac probability distribution function, thermal generation intrinsic semiconductors, mass action law<br>2. Learn Energy band structure of materials, Electrical neutrality, calculation of fermi level – hole – electron, mobility drift current, conductivity diffusion current Hall effect, band structure of PN Junction, temperature depend in characteristics.<br>3. Learn Calculation of transition and diffusion capacitance, characteristics of varactor diode, avalanche and zener breakdown, effect of temperature and breakdown, Effect of light and tunneling effect.<br>4. Learn junction transistors, current components, gain-with modulation Breakdown characteristics, Ebers–Moll model, Transistor switching times. Characteristics of JFET, pinch off voltage and drain current MOSFETs<br>5. Learn charectersistics of ohmic contacts, semiconductor powercontrol devices such as UJT, SCR Triac and Diac. | The students should be able to:<br>6. Calibrate force and motion of a charge in electric and magnetic fields, carrier densities in intrinsic and extrinsic semiconductor, implementing mass action law.<br>7. Apply law of electrical neutrality calculation of location of Fermi level and hole densities in extrinsic semiconductors as well as mobility, drift current, diffusion current, use of continuity equation and hall effect, evaluate the conduction of PN Junction as a function of temperature.<br>8. Evaluate the characteristics of given diode for application<br>9. Analyze the characteristics of given transistor, at critical voltage and current values as required by the applications.<br>10. Evaluate ohmic contact characteristics, power control device characteristics and application |

**UNIT I ELECTRON BALLISTICS AND INTRINSIC SEMICONDUCTORS 9**

Force on charge in electric field – Motion of Charge in uniform and time varying electric fields – Force on a moving charge in a magnetic field – calculation of cyclotron frequency – calculation of electrostatic and magnetic deflection sensitivity.

Energy band structure of conductors, semiconductors and insulators – Density distribution of available energy states in semiconductors – Fermi- Dirac probability distribution function at different temperatures – Thermal generation of carriers – Calculation of electron and hole densities in intrinsic semiconductors – Intrinsic concentration – Mass Action Law.

**UNIT II EXTRINSIC SEMICONDUCTOR AND PN JUNCTIONS 9**

N and P type semiconductors and their energy band structures – Law of electrical neutrality – Calculation of location of Fermi level and free electron and hole densities in extrinsic semiconductors – Mobility, drift current and conductivity – Diffusion current – Continuity equation - Hall effect.

Band structure of PN Junction – Current Component in a PN Junction – Derivation of diode equation – Temperature dependence of diode characteristics.

**UNIT III SWITCHING CHARACTERISTICS OF PN JUNCTION AND SPECIAL DIODES 9**

Calculation of transition and diffusion capacitance – Varactor diode – charge control description of diode – switching characteristics of diode – Mechanism of avalanche and Zener breakdown – Temperature dependence of breakdown voltages – Backward diode – Tunneling effect in thin barriers Tunnel diode – Photo diode – Light emitting diodes.

**UNIT IV BIPOLAR JUNCTION TRANSISTORS AND FIELD EFFECT TRANSISTORS 9**

Construction of PNP and NPN transistors – BJT current components – Emitter to collector and base to collector current gains – Base width modulation CB and CE characteristics – Breakdown characteristics – Ebers – Moll model – Transistor switching times.

Construction and Characteristics of JFET – Relation between Pinch off Voltage and drain current – Derivation. MOSFET – Enhancement and depletion types.

**UNIT V METAL SEMICONDUCTOR CONTACTS AND POWER CONTROL DEVICES 9**

Metal Semiconductor Contacts - Energy band diagram of metal semiconductor junction Schottky diode and ohmic contacts.

Power control devices: Characteristics and equivalent circuit of UJT - intrinsic stand off ratio. PNPN diode – Two transistor model, SCR, Triac, Diac.

**L = 45, TOTAL = 45**

**TEXT BOOK**

Jacob Millman & Christos C.Halkias, "Electronic Devices and Circuits" Tata McGraw–Hill, 1991 .

**REFERENCES**

1. Nandita Das Gupta and Amitava Das Gupta, Semiconductor Devices – Modeling
2. and Technology, Prentice Hall of India, 2004.
3. Donald A.Neaman," Semiconductor Physics and Devices" 3rd Ed., Tata McGraw-Hill, 2002.

4. S.Salivahanan, N.Sureshkumar and A.Vallavaraj, Electronic Devices and Circuits, TMH, 1998.
5. S.M.Sze, Semiconductor Devices – Physics and Technology, 2nd edn. John Wiley, 2002.
6. Ben G.Streetman and Sanjay Banerjee, Solid State Electronic Devices, Pearson Education 2000.

## ADVANCED RADIATION SYSTEMS

**L T P C**
**3 1 0 4**

| PCS102 | ADVANCED RADIATION SYSTEMS | 4 CREDITS |
|---|---|---|
| **Prerequisite** | Antennas & Propagation | |
| **Goal** | To make the student knowledge be in various types of antennas used in communication | |

| Objectives | Outcomes |
|---|---|
| The course should enable the students to:<br>‘<br>1. Review the fundamentals of E.M. radiation<br>2. Reason for using arrays types and advantages<br>3. Discuss the operative types of Antennas<br>4. Have knowledge about micro strip antennas and their advantages.<br>5. Discuss and appreciate polarization as related to antennas and exploit it. | At the end of the course the students<br>:<br>1.Must become familiar with fundamental and specifications for antennas<br>2. Must become knowledgeable for reasons for going for arrays and their advantages & disadvantages.<br>3. Should have knowledge of several aperture type antennas and their advantages.<br>4. Understand the various micro strip antennas and typical uses for them.<br>5. Familiar with polarization and its utilization in increasing bandwidth. |

**UNIT I CONCEPTS OF RADIATION 9**

Retarded vector potentials – Heuristic approach and Maxwell’s equation approach. The Lorentz gauge condition. Vector potential in Phasor form. Fields radiated by an alternating current element. Total power radiated and radiation resistance. Radiation from Half wave dipole from assumed current distribution. Power radiated in the farfield. Electric vector potential F for a magnetic current source M. Far zone fields due to magnetic source M.

**UNIT II ANTENNA ARRAYS 9**

N element linear arrays – uniform amplitude and spacing. Phased arrays. Directivity ofBroadside and End fire arrays. Three dimensional characteristics. Binomial arrays and Dolph- Tchebycheff arrays. Circular array. Antenna Synthesis- Line source and discretization of continuous sources. Schelkunoff polynomial method. Fourier transform method.

**UNIT III APERTURE ANTENNAS 9**

Magnetic current – Duality. Electric and Magnetic current sheets as sources. Huyghens source. Radiation through an aperture in an absorbing screen. Fraunhoffer and Fresnel diffraction. Cornu Spiral. Complimentary screens and slot antennas. Slot and dipoles as dual antennas. Babinets principle. Fourier transform in aperture antenna theory.

**UNIT IV HORN, MICROSTRIP, REFLECTOR ANTENNAS 9**

E and H plane sectoral Horns. Pyramidal horns. Conical and corrugated Horns. Multimode horns. Phase center. Microstrip antennas – feeding methods. Rectangular patch- Transmission

line model Parabolic Reflector antennas – Prime focus and cassegrain reflectors. Equivalent focal length of Cassegrain antennas. Spillover and taper efficiencies. Optimum illumination.

**UNIT V ANTENNA POLARIZATION 9**

Simple relationship involving spherical triangles. Linear, Elliptical and circular polarization. Development of the Poincare sphere. Representation of the state of polarization in the Poincare sphere. Random polarization – Stokes parameters.

**L=45, T=15, TOTAL= 60**

**TEXT BOOKS:**

1. Balanis, C.A., "Antenna Theory" Wiley, 2003
2. Jordan, E.C., "Electromagnetic waves and Radiating systems". PHI 2003

**REFERENCES:**

1. Krauss, J.D., "Radio Astronomy" McGraw-Hill 1966, (UNIT V)
2. Krauss, J.D.,, Fleisch, D.A., "Electromagnetics" McGraw-Hill,1999

## EMBEDDED SYSTEM DESIGN

**L T P C**
**3 1 0 4**

| **PES102** | **EMBEDDED SYSTEM DESIGN** | **4 CREDITS** |
|---|---|---|
| **Prerequisite** | Nil | |
| **Goal** | The aim of this course is to expose the concepts of Embedded system principles and software development tools and introducing PIC and Motorola microcontrollers and interfacing. | |

| **Objectives** | **Outcomes** |
|---|---|
| The course should enable the students to: | At the end of the course the student should be able to: |
| 1. Review basics in Embedded hardware, | 1. Use of hardware fundamentals. Gates, timing diagram,DMA,interrupts,built - Ins on the microprocessor architecture, |
| 2.Learn basic concepts of design of Embedded software system, | 2. Explain the concept of Tasks,States,Data,Semaphores,more operating system servicesIR in RTOS environment,Basic design using RTOS, |
| 3.Learn the Software architecture and Development tools, | 3. Develop through basic knowledge on the behavior and the characteristics of Round-Robin techniques,Functions,Queue,Host and Target machine and Debugging techniques, |
| 4.Learn the operation of PIC microcontroller and interfacing, | 4. Learn the usage of Architecture,instruction sets of PIC, Loop time subroutine,I/O port expansion,I2C for peripherals chip access,ADC and UART special features, |
| 5. Learn the operation of Embedded Microcomputer systems. | 5. Acquire knowledge on the configuration of Introduction to ARM7 – 2148 – Instructions set,addressing modes, Interfacing methods,ISR,Timing generations and measurements |

**.UNIT I INTRODUCTION : REVIEW OF EMBEDDED HARDWARE 9**

Hardware Fundamentals: Terminology- Gates- Timing Diagram- Microprocessors- Buses- Direct Memory Access- Interrupts- Other Common Parts- Built-Ins on the Microprocessor-Conventions Used on Schematics. Interrupts: Microprocessor Architecture - Interrupts Basics-Shared-Data Problem- Interrupt Latency, Examples of Embedded System.

**UNIT II DESIGN OF EMBEDDED SOFTWARE SYSTEM 9**

Introduction: Tasks and Task States- Tasks and Data- Semaphores and Shared Data. More Operating System Services: Message Queues- Mailboxes and Pipes- Timer Functions- Events- Memory Management- Interrupt Routines in an RTOS Environment, Basic Design Using a Real-Time Operating System.

**UNIT III SOFTWARE ARCHITECTURES AND DEVELOPMENT AND TOOLS 9**

Software Architectures: Round-Robin- Round-Robin with Interrupts- Function-Queue-Scheduling Architecture- Real-Time Operating System Architecture, Development Tools: Host and Target Machines- Linker/Locators for Embedded Software, Debugging Techniques.

**UNIT IV PIC MICROCONTROLLER AND INTERFACING 9**

Introduction- CPU Architecture and Instruction Set- Loop Time Subroutine- Timer2 andInterrupts- Interrupts Timing- I/O Port Expansion- I2C Bus for Peripheral Chip Access- Analog-to- Digital Converter- UART- Special Features.

**UNIT V EMBEDDED MICROCOMPUTER SYSTEMS 9**

Introduction to ARM7 – 2148 – Instructions set - Addressing Modes. Interfacing Methods: Parallel I/O Interface- Parallel Port Interfaces- Memory Interfacing- High Speed I/O interfacing- Analog interfacing, Interrupts, Interrupts Service Routine- Features of Interrupts- Interrupt Vector and Priority, Timing Generation and Measurements: Input Capture- Output Compare- Frequency Measurement, Serial I/O Devices: RS232- RS485.

**L = 45, T = 15, TOTAL= 60**

**TEXT BOOKS:**

1. David E Simon, An Embedded Software Primer, Pearson Education Asia, 2001.
2. John B. Peat man, Design with Microcontroller, Pearson Education Asia, 1998.
3. Jonarthan W. Valvano Brooks/cole,Embedded Micro Computer Systems, Real Time Interfacing, Thomson Learning, 2001.

**REFERENCES:**

1. Burns, Alan and Wellings, Andy, Real-Time Systems and Programming Languages, Second Edition, Harlow: Addison-Wesley-Longman, 1997.
2. Raymond J.A. Bhur and Donald L.Bialey, An Introduction to Real Time Systems: Design to Networking with C/C++, Prentice Hall Inc, NewJersey, 1999.
3. Grehan Moore, and Cyliax, Real Time Programming: A Guide to 32 Bit Embedded Development. Reading: Addison-Wesley-Longman, 1998.
4. Heath, Steve, Embedded Systems Design. Newnes , 1997.

## REAL TIME OPERATING SYSTEM

**L T P C**
**3 1 0 4**

| **PES104** | **REAL TIME OPERATING SYSTEM** | **4 CREDITS** |
|---|---|---|
| Prerequisite | Nil | |
| Goal | To develop in-depth skills in real time operating systems and its application domains | |
| **Objectives** | **Outcomes** | |
| The course should enable the students to:<br><br>1. Know the overview of operating systems.<br><br>2. Know the distributed operating system.<br><br>3. Know the Real Time Models and Languages.<br><br>4. Know the Real Time Kernels principles and standards.<br><br>5. Know the RTOS Application Domains. | At the end of the course the student should be able to:<br><br>1. Understand the concepts of operating system principles, files, processes and structures.<br><br>2. Understand about the distributed operating system.<br><br>3. Understand the concepts of Real Time Models and Languages.<br><br>4. Understand about the Real Time Kernels principles and standards.<br><br>5. Understand about the RTOS Application Domains. | |

**UNIT I REVIEW OF OPERATING SYSTEMS 9**

Basic Principles-system calls-Files-Processes - Design and implementation of processes-Communication between processes - operating system structures.

**UNIT II DISTRIBUTED OPERATING SYSTEMS 9**

Topology-Network Types-Communication-RPC-Client server model-Distributed file systems.

**UNIT III REAL TIME MODELS AND LANGUAGES 9**

Event based - Process based-Graph models - Petrinet models - RTOS tasks - RT scheduling - Interrupt processing-Synchronization - Control blocks-Memory requirements.

**UNIT IV REAL TIME KERNEL 9**

Principles - Polled loop systems - RTOS porting to a target - Comparison and Study of RTOS - VxWorks and mCoS, Introduction to POSIX and OSEK standards.

**UNIT V RTOS AND APPLICATION DOMAINS 9**

RTOS for image processing - Embedded RTOS for voice over IP-RTOS for fault tolerant applications - RTOS for control systems.

**L = 45, T = 15, TOTAL= 60**

**TEXT BOOKS:**

1. Hermann K, "Real time systems-design principles for distributed embedded Applications", kluwer academic, 1995
2. Charles Crowley "operating systems - A design oriented approach" McGraw Hill

**REFERENCES:**

1. RAJ BUHR,DL Beily, "An introduction to real time systems" PHI,1999
2. CM Krishna,Kang G. Shin, "Real time Systems", Mc Graw Hill, 1997
3. Raymond J.A., Donald L Baily, "An introduction to real time operating systems" PHI, 1999

## DIGITAL SIGNAL PROCESSING STRUCTURES FOR VLSI

**L T P C**
**3 1 0 4**

| **PVL203** | **DIGITAL SIGNAL PROCESSING STRUCTURES FOR VLSI** | **4 CREDITS** |
|---|---|---|
| **Prerequisite** | - | |
| **Goal** | The student will get to know the importance of DSP Algorithms and filter design with retiming, pipelining and parallel processing concepts in the field of VLSI design | |
| **Objectives** | **Outcome** | |
| The course should enable the students to<br>1. Study the concept of DSP Algorithms and iteration bound ,pipelining and parallel processing of FIR filters<br>2. Study the concept of retiming, unfolding Algorithms and parallel processing application and Algorithmic strength reduction in filters<br>3. Study the concepts of fast convolution, pipelining and parallel processing of IIR filters<br>4. Study the concept of Scaling and Round off Noise, bit-level arithmetic architectures<br>5.Study the concept of numerical strength reduction, synchronous, wave and asynchronous pipelining | At the end of the course the student should be able to:<br>1.Understand the concepts of DSP Algorithms and iteration bound ,pipelining and parallel processing of FIR filters<br>2.Understand concept of retiming, unfolding Algorithms and parallel processing application, Algorithmic strength reduction in filters<br>3. Understand concept of fast convolution algorithm, pipelining and parallel processing of IIR filters<br>4. Understand the concept of Scaling and Round off Noise, bit-level arithmetic architectures<br>5.Understand the concept of numerical strength reduction, synchronous, wave and asynchronous pipelining | |

**UNIT I INTRODUCTION TO DSP SYSTEMS, PIPELINING AND PARALLEL PROCESSING OF FIR FILTERS 9**

Introduction to DSP systems – Typical DSP algorithms, Data flow and Dependence graphs - critical path, Loop bound, iteration bound, longest path matrix algorithm, Pipelining and Parallel processing of FIR filters, Pipelining and Parallel processing for low power.

**UNIT II RETIMING, ALGORITHMIC STRENGTH REDUCTION 9**

Retiming – definitions and properties, Unfolding – an algorithm for unfolding, properties of unfolding, sample period reduction and parallel processing application, Algorithmic strength reduction in filters and transforms – 2-parallel FIR filter, 2-parallel fast FIR filter, DCT architecture, rank-order filters, Odd-Even merge-sort architecture, parallel rank-order filters

**UNIT III FAST CONVOLUTION, PIPELINING AND PARALLEL PROCESSING OF IIR FILTERS 9**

Fast convolution – Cook-Toom algorithm, modified Cook-Toom algorithm, Pipelined and parallel recursive filters – Look-Ahead pipelining in first-order IIR filters, Look-Ahead pipelining with power-of-2 decomposition, Clustered look-ahead pipelining, Parallel processing of IIR filters, combined pipelining and parallel processing of IIR filters.

**UNIT IV SCALING, ROUND-OFF NOISE, BIT-LEVEL ARITHMETIC ARCHITECTURES 9**

Scaling and round-off noise – scaling operation, round-off noise, state variable description of digital filters, scaling and round-off noise computation, round-off noise in pipelined IIR filters, Bit-level arithmetic architectures – parallel multipliers with sign extension, parallel carry-ripple and carry-save multipliers, Design of Lyon's bit-serial multipliers using Horner's rule, bit-serial FIR filter, CSD representation, CSD multiplication using Horner's rule for precision improvement, Distributed Arithmetic fundamentals and FIR filters

**UNIT V NUMERICAL STRENGTH REDUCTION, SYNCHRONOUS, WAVE AND ASYNCHRONOUS PIPELINING 9**

Numerical strength reduction – sub expression elimination, multiple constant multiplication, iterative matching, synchronous pipelining and clocking styles, clock skew in edge-triggered single phase clocking, two-phase clocking, wave pipelining. Asynchronous pipelining bundled data versus dual rail protocol

**L = 45, T = 15, TOTAL= 60**

**TEXT BOOK**

1.Keshab K. Parhi, " VLSI Digital Signal Processing Systems, Design and implementation ", Wiley, Interscience, 2007.

**REFERENCES:**

1. John G.Proakis, Dimitris G.Manolakis,"Digital Signal Processing" , Prentice Hall of India, 1995

2. Rabiner and Gold - "Theory and Applicatin of Digital Signal Processing" , A Comprehensive,Industrial - Strength DSP REFERENCE. ( 1981).

3.U. Meyer – Baese, " Digital Signal Processing with Field Programmable Gate Arrays", Springer, Second Edition, 2004

## TESTING OF VLSI CIRCUITS

**L T P C**
**3 1 0 4**

| **PVL204** | **TESTING OF VLSI CIRCUITS** | **4 CREDITS** |
|---|---|---|
| **Prerequisite** | - | |
| **Goal** | The student will get to know the importance of testing a design and the cost incurred in testing and the loss for the industry if an IC is untested and released in the market. | |

| **Objectives** | **Outcomes** |
|---|---|
| The course should enable the students to | At the end of the course the student should be able to: |
| 1. Study the need for testing, testing equipment, types of testing and fault modeling, | 1. Understand the role and need of testing, |
| 2. Study the fault in digital circuits, test generation for combination circuits and design of testable combinational circuits, | 2. Understand the fault in digital circuits and able to detect and design testable combinational circuits, |
| 3. Study the concept of testable sequential circuit, memory, ADC and DAC, Mixed circuits and design of testable sequential circuit, | 3. Generate test vectors for sequential circuit and also design of testable sequential circuits, |
| 4. Study the concept of delay, path test and leakage current, | 4. Understand the concept of leakage current and its practical consideration with testing, |
| 5. Study the concept of DFT and scan techniques. | 5. Understand the different scan techniques and DFT concepts. |

**UNIT I VLSI TESTING PROCESS AND FAULT MODELING 9**

Introduction - Need for testing - VLSI Testing Process and Test Equipment - Types of testing - ATE - Parametric testing - Test Economics - Fault Modeling-Stuck at faults, Calculation of DCR and ECR.

**UNIT II TESTING OF COMBINATIONAL CIRCUITS 9**

Faults in Digital circuits-failures and faults, modeling of faults, Temporary faults, Test generation for combinational logic circuits, Testable combinational logic circuit design, Algorithm for true value simulation and for fault simulation.

**UNIT III TESTING OF SEQUENTIAL CIRCUITS 9**

Test generation for sequential circuits, Design of testable sequential circuits, DSP based testing - Static ADC & DAC testing methods- Testable memory design. Analog and mixed signal tests.

**UNIT IV TRANSITION AND DELAY TEST METHODOLOGY 9**

Delay test - Path delay test - Transition faults - delay test methodologies - practical consideration - IDDQ testing - Testing methods - Limitations of IDDQ testing - DFT IDDQ.

**UNIT V SCAN TESTING AND JTAG 9**

DFT - Scan Design - Partial scan design - BIST- TPG for BIST - output response analysis, BIST Architectures- Random Logic BIST - Memory and delay fault BIST - JTAG - System test and core based design.

**L = 45, T=15,TOTAL= 60**

**TEXT BOOK:**

1. Parag.K.Lala “Digital Circuit Testing and Testability” Academic Press

**REFERENCES:**

1. Viswani D.Agarval Michael L.Bushnell, “Essentials of Electronic Testing for Digital Memory & Mixed Signal VLSI Circuit”, Kluwer Academic Publications, 1999
2. Alfred L.Crouch “Design for Test for Digital IC’s And Embedded Core Systems”, - PHI1999.

## VLSI DESIGN AND EMBEDDED SYSTEMS LAB

**L T P C**
**0 0 3 2**

| **PVE205** | **VLSI DESIGN AND EMBEDDED SYSTEMS LAB** | **2 CREDITS** |
|---|---|---|
| **Prerequisite** | NIL | |
| **Goal** | To design Digital System in Verilog and to analyze the CMOS circuit using backend tools.<br>To provide exposure to the students about various microcontroller programming and their interfacing, programming concepts in RTOS environment | |
| **Objectives** | **Outcomes** | |
| The course should enable the students learn about:<br><br>1. To design combinational circuits as synthesizable models in Verilog.<br><br>2. To design sequential circuits as synthesizable models in Verilog.<br><br>3.To learn and analyze the CMOS circuits characteristics using backend tools<br><br>4. Microcontroller programming<br><br>5.RTOS environment | On completion of this course the student should be able to:<br><br>1. Design and implement various digital combinational circuits using Xilinx Simulator.<br><br>2. Design and implement various digital sequential circuits using Xilinx Simulator.<br><br>3. Design and Analysis of CMOS Circuits<br><br>4. Design, simulate and perform interfacing programs using 8051 ,68HC11,PIC and ARM7<br><br>5. Testing RTOS environment and system programming KEIL tools | |

**LIST OF EXPERIMENTS**

1. Design of Combinational circuits

2. Design of Sequential circuits

3. Design of finite state machines based on Mealy and Moore methods

4. Design of NMOS and CMOS Inverters - DC and transient characteristics andswitching times

5. Estimation of Resistance, Capacitance and Inductance

6. Modeling and Simulation of NMOS and CMOS circuits using Spice

7. **MICROCONTROLLER PROGRAMMING**

- Interfacing programs using 68HC11
- Interfacing Programs using 8051 Microcontrollers
- Interfacing with PIC
- Interfacing with ARM7

8**. RTOS ENVIRONMENT**

- Testing RTOS Environment and System Programming
- KEIL tools

**TOTAL=45**

**SEMESTER III**
**PROJECT WORK (PHASE I)**

| L | T | P | C |
|---|---|---|---|
| 0 | 0 | 12 | 6 |

| PVE301 | PROJECT WORK (PHASE I} | 6 CREDITS |
|---|---|---|
| **Prerequisite** | | |
| **Goal** | To develop the student's skills and enable innovation in design and fabrication work from the theoretical and practical skill acquired from the previous semesters. | |

| Objectives | Outcomes |
|---|---|
| The course should enable the students to:<br>1. Select and work on real life application in the field of Electronics & Communication,<br>2. Implement their skills acquired in the previous semesters to practical problems,<br>3. Apply and enhance the knowledge acquired in the related field,<br>4. Make the students come up with new ideas in his area of interest. | At the end of the course the student should be able to:<br>1. Appreciate various aspects of the curriculum which support students in increasing their mastery,<br>2. Get an idea and develop confidence in designing, analyzing and executing the project,<br>3. Develop knowledge of latest trends in fabrication relate their ideas to industrial applications,<br>4. Have complete understanding of making a product. |

**NOTE:**

The objective of the project work is to enable the students onaprojectinvolvingtheoreticalandexperimentalstudiesrelatedtothebranchof study.Everyprojectworkshallhaveaguidewhoisthememberofthefacultyoftheinstitution.Twelve hours perweekshallbeallottedinthetimetableandthistimeshallbeutilizedbythestudentsto receivethedirectionsfromtheguide,onlibraryreading,laboratorywork,computeranalysisorfield workasassignedbytheguideandalsotopresentinperiodicalseminarsontheprogressmadein the project.

Each student will be assigned any one of the following types of project/thesis work:

(a) Industrial case study
(b) Preparation of a feasibility report
(c) Thesis by experimental research, and
(d) Design and development of equipment.

Each report must contain student's own analysis or design presented in the approved format.
Sessional marks will include

(a) Evaluation of the student's progress,
(b) Degree of involvement and participation,

(c) Merit of the project.

A student will have to defend his/her project/thesis and credit will be given on the merits of presentation and viva-voce examination.

**SEMESTER IV**
**PROJECT WORK (PHASE II)**

| L | T | P | C |
|---|---|---|---|
| 0 | 0 | 24 | 12 |

| **PVE401** | **PROJECT WORK (PHASE II)** | **12 CREDITS** |
|---|---|---|
| **Prerequisite** | | |
| **Goal** | To develop the student's skills and enable innovation in design and fabrication work from the theoretical and practical skill acquired from the previous semesters. | |

| **Objectives** | **Outcomes** |
|---|---|
| The course should enable the students to:<br>1. Select and work on real life application in the field of Electronics & Communication,<br>2. Implement their skills acquired in the previous semesters to practical problems,<br>3. Apply and enhance the knowledge acquired in the related field,<br>4. Make the students come up with new ideas in his area of interest. | At the end of the course the student should be able to:<br>1. Appreciate various aspects of the curriculum which support students in increasing their mastery,<br>2. Get an idea and develop confidence in designing, analyzing and executing the project,<br>3. Develop knowledge of latest trends in fabrication relate their ideas to industrial applications,<br>4. Have complete understanding of making a product. |

**NOTE:**

The objective of the project work is to enable the students onaprojectinvolvingtheoreticalandexperimentalstudiesrelatedtothebranchof study.Everyprojectworkshallhaveaguidewhoisthememberofthefacultyoftheinstitution.Twenty four hours perweekshallbeallottedinthetimetableandthistimeshallbeutilizedbythestudentsto receivethedirectionsfromtheguide,onlibraryreading,laboratorywork,computeranalysisorfield workasassignedbytheguideandalsotopresentinperiodicalseminarsontheprogressmadein the project.

Each student will be assigned any one of the following types of project/thesis work:

(a) Industrial case study
(b) Preparation of a feasibility report
(c) Thesis by experimental research, and
(d) Design and development of equipment.

Each report must contain student's own analysis or design presented in the approved format.

Sessional marks will include

(a) Evaluation of the student's progress,
(b) Degree of involvement and participation,
(c) Merit of the project.

A student will have to defend his/her project/thesis and credit will be given on the merits of presentation and viva-voce examination.

## ANALOG VLSI DESIGN

**L T P C**
**3 0 0 3**

| **PVL201** | **ANALOG VLSI DESIGN** | **3 CREDITS** |
|---|---|---|
| **Goal** | The student will get to know an in-depth study of Analog VLSI Signal and Information Processing and Design Methods. | |
| **Objectives** | **Outcomes** | |
| The course should enable the students to<br>1. Study the basics of Analog VLSI Microelectronics and CMOS circuit techniques,<br>2. Study the principles of Continuous-Time Signal Processing and Low-Voltage Signal Processing,<br>3. Study the basics of BiCMOS circuit techniques and Current-Mode Signal Processing,<br>4. Study the principles of Neural Information Processing and Analog VLSI Interconnects,<br>5. Study basics of Sampled-Data Analog Filters and Over-Samples Data Converters. | At the end of the course the student will<br>1. Get introduced to Analog VLSI Microelectronics and the basic techniques of CMOS circuit design,<br>2. Understand the different circuits and methods involved in Continuous-Time Signal Processing and Low-Voltage Signal Processing,<br>3. Understand the basics of BiCMOS circuit techniques and methods of Current-Mode Signal Processing ,<br>4. Understand the models and methods involved in Neural Information Processing and Analog VLSI Interconnects ,<br>5. Understand the different circuits and methods involved in Continuous-Time Signal Processing and Low-Voltage Signal Processing. | |

**UNITI INTRODUCTION TO ANALOG VLSI AND BASIC CMOS CIRCUIT TECHNIQUES** **9**

Introduction to Analog VLSI: VLSI Microelectronics- Mixed-Signal VLSI chips- Potential of Analog VLSI, Basic CMOS circuit Techniques: MOS Models- Current Division Technique- Basic Gain Stage- Limitations- Gain-Boosting Technique- Super MOS Transistor.

**UNIT II CONTINUOUS-TIME SIGNAL PROCESSING AND LOWVOLTAGE SIGNAL PROCESSING 9**

Continuous-Time Signal Processing: Primitive Analog Cells- Linear Voltage-Current Converters- MOS Multipliers- MOS Resistors- Winner-Take-All Circuits- Amplifier-Based Signal Processing, Low-Voltage Signal Processing: CMOS Operational Amplifier Design- Bipolar Operational Amplifier Design.

**UNITIIIBiCMOS CIRCUIT TECHNIQUES AND CURRENT - MODE SIGNAL PROCESSING 9**

BiCMOS Circuit Techniques: Devices and Technology- Basic Analog Sub-circuits, Current-Mode Signal Processing: Continuous-Time Signal Processing- Sampled-Data Signal Processing- Switched-Current Data Converters.

**UNIT IV NEURAL INFORMATION PROCESSING AND ANALOG VLSI INTERCONNECTS 9**

Neural Information Processing: Analog Strong-Inversion Networks- Floating-Gate- Low-Power Neural Networks- CMOS Technology and Models- Design Methodology- Networks. Analog VLSI Interconnects: Physics of Interconnects in VLSI- Scaling of Interconnects- Model for Estimating Circuit Wiring Density- Configurable Architecture for Prototyping Analog Circuits.

**UNIT V SAMPLED-DATA ANALOG FILTERS AND OVER SAMPLED A/D CONVERTERS 9**

Sampled-Data Analog Filters: First-Order SC Circuits- Bilinear Transformation- Second-Order SC Circuits and Cascade Design- Switched-Capacitor Ladder Filters- Synthesis of Switched-Current Filters, Over sampled A/D Converters: Nyquist Rate A/D Converters- Modulators for Oversampled A/D Conversion.

**TOTAL= 45**

**TEXT BOOK:**

1. Mohammed Ismail, Terri Fiez, "Analog VLSI signal and Information processing", McGraw-Hill International Editions, 1994

**REFERENCES:**

1. MalcomR.Haskard, LanC.May, "Analog VLSI Design - NMOS and CMOS"., Prentice Hall,1998
2. Randall L Geiger, Phillip E. Allen, "Noel K.Strader, VLSI Design Techniques for Analog and Digital Circuits", McGraw Hill International Company, 1990
3. Jose E.France, YannisTsividis, "Design of Analog-Digital VLSI Circuits for Telecommunication and signal Processing", Prentice Hall, 1994

## DIGITAL SYSTEM DESIGN WITH PROGRAMMABLE LOGIC

**L T P C**
**3 0 0 3**

| **PVL103** | **DIGITAL SYSTEM DESIGN WITH PROGRAMMABLE LOGIC** | **3 CREDITS** |
|---|---|---|
| **Prerequisite** | - | |
| **Goal** | The student will get the knowledge on design aspects of combinational logic circuits and state machines using PLDs | |
| **Objectives** | **Outcomes** | |
| The course should enable the students to<br>1. Study advanced topics in Boolean Algebra and Programmable Logic Devices,<br>2. Study the design Flow and Multilevel Logic Minimization,<br>3. Study the concepts about Design of FSM,<br>4. Study basic concept in Verilog HDL,<br>5. Study basic concept in VHDL. | At the end of the course the student should be able to:<br>1. Understand the concepts of Boolean Algebra and Programmable Logic Devices,<br>2. Understand concept of design Flow and Multilevel Logic Minimization,<br>3. Understand concept of Design of FSM,<br>4. Write and perform Verilog HDL coding of all digital circuits.,<br>5. Write and perform VHDL coding of all digital circuits. | |

**UNIT I INTRODUCTION TO ADVANCED DIGITAL SYSTEMS 9**

Minimization of Boolean expression, K-Map, QuineMcClusky method, Design of CLC, Multiple output minimization, Design of static hazard free and dynamic hazard free logic circuits, Programmable logic primer : PLA, PAL - PLDs, Programmable Gate Arrays. FPGAs :

Xilinx 3000 series and 4000 series, Altera complex programmable logic devices (CPLDs), Altera flex 10k seriesCPLDs.

**UNIT II FINITE STATE MACHINE 9**

Design of sequential logic circuits, Finite state machines, Mealy machine, Moore Machine, State diagram, State table minimization, State assignment, implementing specified state machine, One hot encoding - SM charts - linked state machine.

**UNIT III FINITE STATE MACHINE 9**

Architectures centered around Non-registered PLDs, State machine design centered around shift registers, One-hot design method, Use of ASMs in one-hot design, Application of one-hot method, System level design-controller- data path and functional partition.

**UNIT IVBASIC CONCEPTS IN Verilog HDL 9**

Basic concepts - Modules instances - operators - data types - Number specification - System tasks and compiler directives - Modules and ports - Gate level modeling - Data flow modeling - Behavioral modeling Advanced Verilog topics : Tasks and functions - useful modeling techniques - Timing and delays - logic synthesis with Verilog HDL - Examples of sequential circuit synthesis.

**UNITBASIC CONCEPTS IN VHDL 9**

Concurrent VHDL: Signal assignment - Transport and inertial delay - objects, classes and type Data types - Generics - Vector assignments, Sequential VHDL.

**TOTAL= 45**

**TEXT BOOKS:**


1. Charles.H.Roth, Jr : Digital Systems Design using VHDL, PWS Publishing Company, 2001.
2. "VHDL for Designers" by Stefan Sjoholm and LennartLindh.
3. M.Bolton : Digital System Design with Programmable Logic, Addition Wesly . (1990)


**REFERENCES:**


1. P.K.Chan& S. Mourd : Digital Design using Field programmable Gate Array, (1994), Prentice Hall (PTR).
2. William I.Fletcher : An Egineering Approach to Digital Design , Prentice Hall of India, 1996.
3. R.F. Tinder : Engineering Digital Design, (2000), Academic Press.
4. N.N Biswas : Logic Design Theory , Prentice Hall of India, 1993.
5. 5.J.V. Oldfield &R.C.Dorf : Field Programmable Gate Array, (1995), John-wiley

## VLSI TECHNOLOGY

**L T P C**
**3 0 0 3**

| PVL701 | VLSI TECHNOLOGY | 3 CREDITS |
|---|---|---|
| **Prerequisite** | | |
| **Goal** | To understand different techniques and methods involved in the Fabrication of semiconductor devices used in VLSI Technology . | |
| **Objectives** | **Outcomes** | |
| The course should enable the students to:<br><br>(i) Study basics of crystal growth, wafer preparation, epitaxy and oxidation,<br><br>(ii) Study the Lithography and plasma etching,<br><br>(iii) Study the deposition, diffusion , Ion implantation Techniques,<br><br>(iv) Study the IC fabrication of different MOS devices,<br><br>(v Study the Assembly Techniques and Packaging of VLSI Devices. | At the end of the course the student should be able to:<br><br>(i) Understand the different methods of crystal growth, many epitaxial methods and oxidation techniques in the process of wafer preparation,<br><br>(ii) Understand the different types of lithography and various mechanisms of etching and the equipments used ,<br><br>(iii)Understand various deposition techniques, a detailed view of diffusion mechanism and the metallization process in fabrication,<br><br>(iv)Understand the IC technology in various MOS devices such as NMOS, CMOS, as well as Bipolar IC and MOS Memory Devices,<br><br>(v) Understand the VLSI assembly Technology, Package Types and Package fabrication technology. | |
| | | |

**UNIT I CRYSTAL GROWTH, WAFER PREPARATION, EPITAXY**

**AND OXIDATION** **9**

Electronic Grade Silicon- Czochralski Crystal Growing- Silicon Shaping- Processing Consideration- Vapor Phase Epitaxy- Molecular Beam Epitaxy- Silicon on Insulators- Epitaxial Evaluation - Growth Mechanism and Kinetics- Thin Oxides - Oxidation Techniques and Systems-Oxide Properties- Redistribution of Dopants at interface- Oxidation of Poly Silicon- Oxidation Induced Defects.

**UNIT II LITHOGRAPHY AND RELATIVE PLASMA ETCHING** **9**

Optical Lithography- Electron Lithography- X-Ray Lithography-Plasma Properties- Feature Size Control and Anisotropic Etch Mechanism- Relative Plasma Etching Techniques and Equipments.

**UNIT III DEPOSITION, DIFFUSION, ION IMPLANTATION AND METALISATION** **9**

Deposition Processes- Polisilicon- Plasma Assisted Deposition- Models of Diffusion in Solids- Fick's One Dimensional Diffusion Equation- Atomic Diffusion Mechanism- Measurement Techniques- Range Theory- Implantation Equipment- Annealing Shalloe junction- High Energy Implantation- Physical Vapor Deposition- Patterning.

**UNIT IV PROCESS SIMULATION AND VLSI PROCESS INTEGRATION** **9**

Ion Implantation- Diffusion and Oxidation- Epitaxy- Etching and Deposition- NMOS IC Technology- CMOS IC Technology - MOS Memory IC Technology- Biploar IC Technology- IC Fabrication.

**UNIT V ANALYTICAL, ASSEMBLY TECHNIQUES AND PACKAGING OF VLSI DEVICES** **9**

Analytical Beams- Beams Specimen Interaction- Chemical Methods- Package Types baking Design Consideration- VLSI Assembly Technology- Package Fabrication Technology.

**L = 45, TOTAL= 45**

**TEXT BOOK:**

1. S.M.Sze, "VLSI Technology" ,McGRAW HILL second Edition International Edition, 1998, Electrical and Electronic Engineering Series 1998

**REFERENCES:**

1. Duoglas A Puchnell and Kamran Eshranghian, "Basic VLSI Design" Prentice Hall of India, New Delhi, Third edition,1994

2. Duoglas A Puchnell and Kamran Eshranghian, "Basic VLSI Design" Prentice Hall of India, New Delhi, Third edition,1994

3. Wayne Wolf, "Modern VLSI Design: IP based Design, Pearson Education, 4$^{th}$ed, 2008

## LOW POWER VLSI DESIGN

**L T P C**
**3 0 0 3**

| PVL703 | LOW POWER VLSI DESIGN | 3 CREDIT |
|---|---|---|
| **Prerequisite** | | |
| **Goal** | To understand the basics and advanced techniques in low power design, reduction in power dissipation, reduction in size, cost and etc. | |
| **Objectives** | **Outcomes** | |
| The course should enable the students to<br><br>1. Learn the design of low power ICS<br><br>2. Learn the Power Dissipation mechanism in various devices,<br><br>3. Learn the Design and test for Low power devices and optimization techniques involved in the design,<br><br>4. Learn the design and test for low power memory devices,<br><br>5. Learn the Software design for low power devices. | At the end of the course the student should be able to:<br><br>1. Understand the sources of power dissipation, power dissipation in MOSFET devices,<br><br>2. Understand the calculation for signal activity estimation and estimation of power in circuit level,<br><br>3. Understand the logic level and circuit optimization for low power circuits. Also to understand the design and testing of low power CMOS circuits,<br><br>4. Understand the low power static RAM Architectures, designing and testing of memory devices with low power dissipation,<br><br>5. Understand the sources of software power dissipation, software power estimation and its design. | |

**UNIT I DESIGN OF LOW POWER ICs** **9**

Introduction - Sources of power dissipation - Design for low power - Power dissipation in MOSFET devices - Power dissipation in CMOS -Low power design limits

**UNIT II PROBABILITY CALCULATION AND ESTIMATION OF POWER IN CIRCUIT LEVEL 9**

Signal probability calculation-Probabilistic calculation for signal activity estimation-Statistical techniques for estimating average power in combinational and sequential circuits-Estimation of glitching power -Sensitivity analysis-Estimation of power in circuit level and IT based approaches.

**UNIT III DESIGN AND TEST FOR LOW POWER CMOS CIRCUITS 9**

Synthesis for low power - Behavioral level transforms-Logic level optimization for low power circuit level optimization and transforms-Future directions-design and test of low power CMOS circuits-Circuit design style-Leakage current in deep sub micrometer device design issues-low voltage design techniques.

**UNIT IV SYNTHESIS FOR LOW POWER & TEST OF LOW VOLTAG CMOS CIRCUITS 9**

Low power static RAM architectures- MOS static RAM memory cell -Organization of SRAMs-Reducing voltage swing, power - Low energy computing-Energy dissipation in transistor channels-Energy recovery circuit design - Design with partially reversible logic-Supply clock generation.

**UNIT V SOFTWARE DESIGN FOR LOW POWER 9**

Software design for low power - Sources of software power dissipation - Software power estimation - Software power optimization - Automated low power code generation - Co design for low power.

**L = 45, TOTAL=45**

**TEXT BOOK:**

1. KaushikRoy ,Sharat C. Prasad "Low power CMOS VLSI circuit design" "A Wiley Inter science Publications". (1987)

**REFERENCE:**

1. Gary Yeap "Practical Low Power Digital VLSI Design", 1997

## PHYSICAL DESIGN OF VLSI CIRCUITS

**L T P C**
**3 0 0 3**

| **PVL705** | **PHYSICAL DESIGN OF VLSI CIRCUITS** | **3 CREDITS** |
|---|---|---|
| **Prerequisite** | - | |
| **Goal** | To familiarize the standard algorithms for VLSI Physical design automation. | |

| **Objectives** | **Outcomes** |
|---|---|
| The course should enable the students to<br>1. Study the concept of VLSI design automation tools,<br>2. Study the concept of layout, placement and routing mechanism,<br>3. Study the concept of floor planning and routing,<br>4. Study the concept of simulation and logic synthesis,<br>5. Study the concept of high level synthesis and scheduling concepts. | At the end of the course the student should be able to:<br>1. Understand the concept of design at different levels and the tools associated at each level,<br>2. Understand the concept of layout, placement and routing concepts with the algorithms,<br>3. Understand the concept of floor planning and routing algorithm,<br>4. Understand the concept of design at gate level and switch level simulation and synthesis,<br>5. Understand the hardware for high level synthesis and the scheduling algorithm. |

**UNIT I VLSI DESIGN AUTOMATION TOOLS 9**

Algorithms and System Design- Structural and Logic Design- Transistor Level Design- Layout Design- Verification Methods- Design Management Tools.

**UNIT II LAYOUT COMPACTION- PLACEMENT AND ROUTING 9**

Design Rules- Symbolic Layout- Application of Compaction- Formulation Methods- Algorithms for Constrained Graph Compaction- Circuit Representation- Wire Length Estimation- Placement Algorithms- Partitioning Algorithms.

**UNIT III FLOOR PLANNING AND ROUTING 9**

Floor Planning concepts- Shape Functions and Floor Planning Sizing- Local Routing- Area Routing- Channel Routing- Global Routing - Global Routing and its Algorithms.

**UNIT IV SIMULATION AND LOGIC SYNTHESIS 9**

Gate Level and Switch Level Modeling and Simulation- Introduction to Combinational Logic Synthesis. ROBDD Principles- Implementation- Construction and Manipulation, Two Level Logic Synthesis.

**UNIT V HIGH-LEVEL SYNTHESIS 9**

Hardware Model for High Level Synthesis- Internal Representation of Input Algorithms- Allocation- Assignment and Scheduling, Scheduling Algorithms- Aspects of Assignment.High Level Transformation.

**L = 45, TOTAL= 45**

**TEXT BOOKS:**

1. S.H. GEREZ: “Algorithms for VLSI Design Automation
2. K.K PARHI : “VLSI Digital Signal processing” . (1999), John-wiley

**REFERENCES:**

1. N.A. SHERWANI: “Algorithms for VLSI Physical Design Automation”, John Wiley, 1998
2. S.M SAIT & H.YOUSSEF: “VLSI Physical Design Automation”, World Science, 1999
3. M. SARRAFZADEH: “ Introduction to VLSI Physical Design”, McGraw Hill (IE),1996

## ADVANCED MICROPROCESSOR

**L T P C**
**3 0 0 3**

| **PES103** | **ADVANCED MICROPROCESSOR** | **3 CREDITS** |
|---|---|---|
| **Prerequisite** | Nil | |
| **Goal** | The aim of this course is to give an in depth knowledge on Advanced Microprocessor | |

| **Objectives** | **Outcomes** |
|---|---|
| The course should enable the students to: | At the end of the course the student should be able to: |
| 1.Understand the use of 16/32 bit Microprocessor | 1. Gain basics of Organization of 8086,80286,80386,80486, Minimum maximum mode, pipeline architecture, addressing modes, memory registration, segmentation, Bus structure and timing, expectation handling, |
| 2.Understand about Assembly level programming | 2. Explain the concept of Assembly level programming of 8086, Instruction types, Macros and Byte string manipulation |
| 3.Understand the Operation of Digital interfacing | 3. Develop through basic knowledge on the behavior and the characteristics Programming parallel ports, Keypad interfacing alphaneumeric display, interfacing high power devices, optical motor shaft encoder, sensor and transducers, convertors and 8086 based control systems |
| 4.Understand the Operation Multiprocessor configuration and introduction to Microprogrammable microprocessors | 4.Learn the usage of Queue status and lock facility,8086/8088 based multiprocessing system,8087 NDP,8089,Pentium 4 |

| | |
|---|---|
| 5. Learn about High performance RISC Architecture. | processor,organization of bit slice processor for microprogrammed machines,<br><br>5.Acquire knowledge on the configuration of ARM 7 Organization and implementation, instruction sets, Basic ARM 7 ALP, ARM CPU cores.<br>. |

**UNIT I 16/ 32 BIT MICROPROCESSOR 9**

Organization of 8086, 80286,80386,80486 microprocessors - Minimum maximum mode - Pipeline Architecture - Registers - Addressing modes - Memory Registration - Memory Segmentation - Instruction set of 8086 - Bus structure and timing - exception handling.

**UNIT II ASSEMBLY LANGUAGE PROGRAMMING 9**

Assembly language programming of 8086 microprocessor - Data transfer instruction - Arithmetic instruction - Branch instructions - Loop instructions - NOP and HALT instructions - Flag manipulation instructions - Logical instructions - Shift and rotate instructions - linking and relocation - stacks procedure - Interrupts and interrupt routines - Macros - Byte and string manipulations.

**UNIT III DIGITAL INTERFACING 9**

Programming Parallel ports - Handshake input/output - interfacing a microprocessor to a keyboard, interfacing to alphanumeric displays, interfacing a microcomputer to high power devices, Optical motor shaft encoders - Sensors and Transducers - D/A converter operations, interfacing & applications- A/D converter Specifications, types & interfacing, A 8086 based process control system.

**UNIT IV MULTIPROCESSOR CONFIGURATIONS, ADVANCED MICROPROCESSOR ARCHITECTURE, INTRODUCTION TO THE MICROPROGRAMMABLE MICROPROCESSORS 9**

Queue status and lock facilities - 8086 / 8088 based multiprocessing system, 8087 numeric data processor, 8089 I/O processor. Introduction to Motorola 68HC11 processor, Pentium4 Microprocessor, Architecture, Instruction set and addressing modes, Organization of bit-slice processor, bit-slice processor architecture for micro-programmed machines.

**UNIT V HIGH PERFORMANCE RISC ARCHITECTURE 9**

ARM: The ARM7 architecture – ARM7 organization and implementation - The ARM7 instruction set - The thumb instruction set - Basic ARM7 Assembly language program - ARM CPU cores.

**TOTAL=45**

**TEXT BOOKS:**

1. Barry B. Brey, "The Intel Microprocessors Architecture, Programming and Interfacing", PHI, 2002 (UNIT I,II,III)
2. Hall.D.V, "Microprocessor and Interfacing: Programming and hardware", McGraw Hill Book Company, New York, 1988 (UNIT III)
3.Liu.Y and Gibson. G. A., "Microcomputer systems: The 8086/ 8088 family: Architecture, Programming and design", Prentice Hall of India Pvt. Ltd, M.D. (1979) (UNIT IV).
4. John Mick and Jim Brick, "Bit-slice Microprocessor Design",*McGraw-Hill*, 1980 (UNIT IV).
5. SteaveFurber, "ARM system - on - chip architecture", Addison Wesley, 2000. (UNIT V)

**REFERENCES:**

1. Daniel Tabak, "Advanced Microprocessors", McGraw Hill. Inc., 1995
2. James L. Antonakos, "The Pentium Microprocessor", Pearson Education, 1997
3. James L Antonakos, "An Introduction to the Intel family of Microprocessors", Pearson Education, 1999

## SOFTWARE TECHNOLOGY FOR EMBEDDED SYSTEMS

**L T P C**
**3 0 0 3**

| **PES202** | **SOFTWARE TECHNOLOGY FOR EMBEDDED SYSTEMS** | **3 CREDITS** |
|---|---|---|
| **Prerequisite** | Nil | |
| **Goal** | The aim of this course is to give an in depth knowledge on Embedded control systems | |

| **Objectives** | **Outcomes** |
|---|---|
| The course should enable the students to: | At the end of the course the student should be able to: |
| 1. Learn about the introduction to data representation, | 1. know Data representations,2s complement, fixed point and floating point numbers, low level programming in c, primitive data types, functions, recursive functions, pointers, structures, unions, dynamic memory allocations ,file handling, linked list, |
| 2. Learn about Programming in assembly, | 2.Know the concept of C and ALP, register usage conventions, addressing options, procedure call and return, parameter passing, retrieving parameter, pass by value, threads, preemptive kernels, system timer scheduling, |
| 3. Learn the Object oriented analysis, | 3.Develop through basic knowledge on the design, object model with case model, key |

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| | strategy, UML basics, |
| 4. Learn about UML, | 4.Know the usage of behavior, UML chart, timing and sequence diagram, event hierarchies, operations, design in UML concurrency design, |
| 5. Learn about software and hardware partitioning. | 5.Know about co-design overview, co simulation, Re-configurable computing, SOC,IP cores, low power real time embedded systems, on chip networking |

**UNIT I INTRODUCTION TO DATA REPRESENTATION 9**

Data representation - Twos complement, fixed point and floating point number formats – Low level programming in C - Primitive data types - Functions - recursive functions - Pointers – Structures - Unions - Dynamic memory allocation - File handling - Linked lists.

**UNIT II PROGRAMMING IN ASSEMBLY 9**

C and assembly - Programming in assembly - Register usage conventions - Typical use of addressing options - Instruction sequencing - Procedure call and return - Parameter passing - Retrieving parameters - Everything in pass by value - Temporary variables - threads – preemptive kernels - system timer – scheduling.

**UNIT III OBJECT ORIENTED ANALYSIS 9**

Object oriented analysis and design- Connecting the object model with the use case model - Key strategies for object identification - UML basics.

**UNIT IV UML 9**

Object state behavior - UML state charts - Role of scenarios in the definition of behavior - Timing diagrams - Sequence diagrams - Event hierarchies - types and strategies of operations - Architectural design in UML concurrency design - threads in UML.

**UNIT V SOFTWARE AND HARDWARE PARTITIONING 9**

Software / Hardware partitioning - Co design overview - Co simulation, synthesis and verifications - Re-configurable computing - System on Chip (SoC) and IP cores - Low-Power RT Embedded Systems - On-chip Networking.

**L = 45, T=15, TOTAL=60**

**TEXT BOOKS:**

1. Bruce powel Douglas, “Real time UML, second edition: Developing efficient objects for embedded systems (The Addison Wesley Object technology series)”. 2nd edition 1999, Addison Wesley

2. Hassan Gomma, ‘Designing concurrent, distributed, and real time applications with

UML,2001
3. Daniel W.Lewis, fundamentals of embedded software where C and assembly meet" PHI 2002

## EMBEDDED NETWORKING

**L T P C**
**3 0 0 3**

| **PES705** | **EMBEDDED NETWORKING** | **3 CREDITS** |
|---|---|---|
| Prerequisite | Nil | |
| Goal | To provide basic knowledge about the embedded networking protocols. | |
| **Objectives** | **Outcomes** | |
| The course should enable the students to:<br>1.Understand the serial andparallel communication protocols.<br>2. Understand the application development using USB and CAN bus for PIC micro controller.<br>3. Understand the Ethernet protocols.<br>4. Understandthe application development using embedded Ethernet for rabbit processors. | At the end of the course the student should be able to:<br>1. Know the concepts of embedded serial communication and parallel communication protocols.<br>2. Know about the application development using USB and CAN bus with C programming for PIC- 18 microcontroller<br>3. Know the concepts of Ethernet protocols and controllers.<br>4. Know the concepts of real time development of embedded Ethernet protocols for rabbit processors. | |

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| 5. Understand the wireless sensor network communication protocols. | 5. Know the wireless embedded networking protocols concepts. |

**UNITI EMBEDDEDCOMMUNICATIONPROTOCOLS 8**

Embedded Networking: Introduction – Serial/Parallel Communication –Serial communicationprotocols-RS232standard–RS485–SynchronousSerialProtocols- Serial PeripheralInterface(SPI)–InterIntegratedCircuits($I^2C$)–PCParallelport programming - ISA/PCIBusprotocols–Firewire

**UNITII USBANDCANBUS 10**

USBbus–Introduction –Speed Identification onthebus–USBStates–USBbus communication: Packets –Data flow types –Enumeration –Descriptors –PIC 18, MicrocontrollerUSBInterface–CPrograms–CANBus–Introduction- Frames–Bit stuffing– Typesoferrors–NominalBitTiming–PICmicrocontrollerCANInterface–A simpleapplicationwithCAN.

**UNITIII ETHERNETBASICS 9**

Elementsofanetwork–InsideEthernet–BuildingaNetwork:Hardwareoptions– Cables, Connectionsandnetworkspeed–Designchoices:Selectingcomponents– EthernetControllers– Usingtheinternetinlocalandinternetcommunications–Inside theInternet protocol

**UNITIV EMBEDDEDETHERNET 9**

ExchangingmessagesusingUDPandTCP–ServingwebpageswithDynamicData– Servingwebpagesthatrespondtouser Input–EmailforEmbeddedSystems–Using FTP– KeepingDevicesandNetworksecure.

**UNITV WIRELESSEMBEDDEDNETWORKING 9**

Wireless sensor networks – Introduction – Applications – Network Topology – Localization– TimeSynchronization-EnergyefficientMACprotocols–SMAC–Energy efficient androbust routing–Data Centricrouting

**TOTAL=45**

**REFERENCES:**


1. FrankVahid,Givargis‘EmbeddedSystemsDesign:AUnified Hardware/SoftwareIntroduction’,Wiley Publications, 2002
2. JanAxelson,‘Parallel Port Complete’,Penram publications, 2006
3. DoganIbrahim, ‘AdvancedPICmicrocontroller projectsinC’, Elsevier2008
4. JanAxelson‘Embedded Ethernet andInternetComplete’, Penram Publications, 2007
5. BhaskarKrishnamachari,‘Networkingwirelesssensors’, Cambridgepress 2005

## EMBEDDED CONTROL SYSTEMS

**L T P C**
**3 0 0 3**

| **PES204** | **EMBEDDED CONTROL SYSTEMS** | **3 CREDITS** |
|---|---|---|
| **Prerequisite** | Nil | |
| **Goal** | The aim of this course is to give an in depth knowledge on Embedded control systems | |

| **Objectives** | **Outcomes** |
|---|---|
| The course should enable the students to: | At the end of the course the student should be able to: |
| 1.Learn about the peripherals interface basics and operation, | 1. Gain knowledge on controlling hardware and software,data lines,numbering systems,address lines,bit masking,PPI,Switch input detection, |
| 2. Learn about interfacing and programming Input output devices, | 2.Know the concept of Keypad scanning algorithm,Multiplexed LED displays,LCD module display,time of day clock,Timer manager,ISR,PWM |
| 3. Learn the Operation of DAC and ADC conversions, | 3.Develop through basic knowledge on the behavior and the characteristics of ADC and DAC working principles,Analog signal measurements,multi channel data |

| | |
|---|---|
| 4. Learn the Operation of Asynchronous serial communication,<br><br>5. Learn about Case studies. | acquisition,auto port detection,recording and playback of voice,<br><br>4.Learn the usage of Asynchronous serial communication,RS-232,485,sending and receiving data,serial ports on PC,Low level PC I/O module,buffered serial I/O,<br><br>5.Acquire knowledge on the Controlling motors,H-bridge,Telephonic systems,burger alarms and fire alarms. |

**UNIT I INTRODUCTION** **9**

Controlling the hardware with software - Data lines - Numbering systems- Address lines - Ports - Schematic representation - Bit masking - Programmable peripheral interface- switch input detection.

**UNIT II INPUT-OUTPUT DEVICES** **9**

Keyboard basics- Keyboard scanning algorithm - Multiplexed LED displays- character LCD modules- LCD module display-configuration- time of day clock-timer manager-interrupts – Interrupt service routines- Interrupt vector or dispatch table multiple point -Interrupt driven pulse width modulation.

**UNIT III D/A and A/D CONVERSION** **9**

D/A and A/D converters and its working principles - Interrupts in analog signal measurement - Multi channel data acquisition. - Auto port detection - recording and playing back voice.

**UNIT IV ASYNCHRONOUS SERIAL COMMUNICATION** **9**

Asynchronous serial communication - RS 232 - RS 485 - Sending and receiving data – Serial ports on PC - Low level PC serial I/O module - Buffered serial I/O.

**UNIT V CASE STUDIES** **9**

Controlling motors - bi-directional - control of motors- H bridge - Telephonic systems – Burger alarms- Fire alarms

**L = 45, TOTAL=45**

**TEXT BOOKS:**

1. Jean J Labrosse, “Embedded System Building Blocks: Complete and Ready to use modules in C” , the publisher , Paul Temme, 1999

2. Ball SR “Embedded microprocessor system - Real world design, Prentice Hall , 1996

**REFERENCES:**

1. Hermann. K “Real Time systems- Design for distributed Embedded Application”, kluwerAcdemic , 1997
2. Daniel W Lewis, “Fundamentals of Embedded software where C and Assembly meet” PHI 2002

## ADVANCED COMPUTER ARCHITECTURE

**L T P C**
**3 0 0 3**

| **PCE720** | **ADVANCED COMPUTER ARCHITECTURE** | **3 CREDITS** |
|---|---|---|
| **Prerequisite** | - | |
| **Goal** | The student will get a balanced study of the theory, Technology and architecture of advanced computer systems. It introduces the issues in designing and using high performance parallel computers. | |
| **Objectives** | **Outcomes** | |

| The course should enable the students to | At the end of the course the student should be able to: |
|---|---|
| 1. Study the uni processor and parallel processor architecture | 1. Understand the different processor architectures and applications |
| 2. Study the parallel computer models and performance metrics | 2. Understand the parallel computer models and performance metrics, measures and approaches. |
| 3. Study the concept of Processors and memory Hierarchy | 3. Understand the Processors and memory Hierarchy and bus structure. |
| 4. Study the concept of Pipelining and super scalar techniques | 4. Understand the concept of Pipelining and super scalar techniques |
| 5. Study the concepts of multiprocessors and compound vector processing | 5. Understand the concept of multiprocessors and compound vector processing principles. |

**UNIT I UNIPROCESSOR AND PARALLEL COMPUTER STRUCTURE 9**

Basic Uniprocessor Architecture - Parallel processing Mechanisms- Balancing of Subsystem band width- Parallel Computer structure- Architectural classifications- Parallel processing applications.

**UNIT II PARALLEL COMPUTER MODELS AND PERFORMANCE 9**

Parallel Computer Models - Multi processing and Multi computers- Multi vector and SIMD Computers - PRAM and VLSI Models. Principles of Scalable Performance - Performance Metrics and measures- Speedup Performance laws- Scalability Analysis and Approaches.

**UNIT III MEMORY 9**

Processors and memory Hierarchy- Advanced Processor Technology-Super scalar and Vector processors- Memory hierarchy technology- Virtual memory Technology. Bus- cache- and shared memory- Backplane Bus Structure- Cache memory organizations- Shared memory organizations.

**UNIT IV DESIGN AND PIPELINING 9**

Pipelining and super scalar techniques- Linear pipe line Processors- Non linear pipeline Processors- Instruction pipeline design- Arithmetic pipeline design- Super scalar and super pipeline design.

**UNIT V MULTIPROCESSOR AND COMPOUND VECTOR PROCESSING 9**

Multi processors and Multi computers- Multi processor system interconnects- Cache coherence and Synchronization Mechanism- Message passing mechanisms Multi vector and SIMD

Computers- Vector processing principles- Compound vector processing-SIMD Computer organizations.

**L = 45, TOTAL= 45**

**REFERENCES:**

1. A Kai Hwang, Advanced Computer Architecture - Kai Hwang, McGraw-Hill, Inc - 1987
2. Kai Hwang and Faye A. Briggs Computer Architecture and Parallel Processing, McGraw - Hill(1989.)
3. Rafiquzzaman, and Chandra -Modern computer Architecture-West Publishing Company, 1989
4. Morris Mano -Computer system Organization- Prentice Hall of India, 3rd ed,(1993.)
5. Andrew s. Tannenbaum -Computer Organization -Prentice Hall,(1991)

## PCS712 - COGNITIVE RADIO

**L T P C**

**3 0 0 3**

**UNIT I : INTRODUCTION TO SDR** **9**

Software Radio aspects, The Need for Software Radios, Characteristics and Benefits of a Software Radio, DesignPrinciples of a Software RadioDefinitions and potential benefits, Role of SDR, Features of SDR, software radio architecture evolution – foundations, technologytradeoffs and architecture implications.

**UNIT II: SDR ARCHITECTURE** **9**

Essential functions of the software radio- Radio architecture evolution, canonical SDR architecture, software radio overview,open architecture software tools, architecture goals, top level component topology, computational properties of functionalcomponents, interface topologies among plug and play modules, architecture partitions.

**UNITIII : INTRODUCTION TO COGNITIVE RADIOS 9**

Marking radio self-aware, Aware, Adaptive & cognitive radios, the cognition cycle, organization of cognition tasks, structuringknowledge for cognition tasks–concepts, architecture, design considerations, , Ultra wide band C shaped monopole Antenna for Cognitive Radio.

**UNIT IV : COGNITIVE RADIO ARCHITECTURE 9**

Primary Cognitive Radio functions, Behaviors, Components, prior knowledge taxonomy, observe phase data structures, Radio Procedure Knowledge Encapsulation, components oforient, plan, decide phases, act phase knowledge representation, design rules.

**UNIT V : NEXT GENERATION WIRELESS NETWORKS 9**

The XG Network architecture, spectrum sensing-Overview – Classification - Matched filter – waveform based sensing – cyclostationary basedsensing,spectrum management, spectrum mobility,spectrum sharing, upper layer issues, cross – layer design.

**TOTAL: 45 PERIODS**

**REFERENCES:**

1.Alexander M. Wyglinski, Maziar Nekovee, And Y. Thomas Hou, " Cognitive Radio Communications And Networks - Principles And Practice", Elsevier Inc. , 2010.

2. "E. Biglieri, A.J. Goldsmith., L.J. Greenstein, N.B. Mandayam, H.V. Poor, Principles of Cognitive Radio", Cambridge University Press, 2013.

3. Kwang-Cheng Chen and Ramjee Prasad, " Cognitive Radio Networks" , John Wiley & Sons, Ltd, 2009.

4. Khattab, Ahmed, Perkins, Dmitri, Bayoumi, Magdy, "Cognitive Radio Networks - From Theory to Practice", Springer Series: Analog Circuits and Signal Processing, 2009.

5. J. Mitola, " Cognitive Radio: An Integrated Agent Architecture for software defined radio", Doctor of Technology thesis, Royal Inst. Technology, Sweden 2000.

6. Simon Haykin, "Cognitive Radio: Brain –empowered wireless communications", IEEE Journal on selected areas in communications, Feb 2005.

7. Ian F. Akyildiz, Won – Yeol Lee, Mehmet C. Vuran, Shantidev Mohanty, “ NeXt generation /dynamic spectrum access / cognitive radio wireless networks: A Survey ElsevierComputer Networks, May 2006.