HINDUSTAN UNIVERSITY
HINDUSTAN INSTITUTE OF TECHNOLOGY & SCIENCE
(Estd. u/s 3 of the UGC Act, 1956)
Padur, Kancheepuram District - 603 103.

DEPARTMENT OF
ELECTRICAL AND ELECTRONICS ENGINEERING

Regulations Curriculum and Syllabus 2013

M.Tech.
APPLIED ELECTRONICS

ACADEMIC REGULATIONS
(M.TECH./ M.B.A. / M.C.A.) (Full - Time / Part - Time)
(Effective 2013-14)

1. Vision, Mission and Objectives

1.1 The Vision of the Institute is "To make every man a success and no man a failure".

In order to progress towards the vision, the Institute has identified itself with a mission to provide every individual with a conducive environment suitable to achieve his / her career goals, with a strong emphasis on personality development, and to offer quality education in all spheres of engineering, technology, applied sciences and management, without compromising on the quality and code of ethics.

1.2 Further, the institute always strives

- To train our students with the latest and the best in the rapidly changing fields of Engineering, Technology, Management, Science & Humanities.
- To develop the students with a global outlook possessing, state of the art skills, capable of taking up challenging responsibilities in the respective fields.
- To mould our students as citizens with moral, ethical and social values so as to fulfill their obligations to the nation and the society.
- To promote research in the field of science, Humanities, Engineering, Technology and allied branches.

1.3 Our aims and objectives are focused on

- Providing world class education in engineering, technology, applied science and management.
- Keeping pace with the ever changing technological scenario to help our students to gain proper direction to emerge as competent professionals fully aware of their commitment to the society and nation.
- To inculcate a flair for research, development and entrepreneurship.

2. Admission

2.1 The admission policy and procedure shall be decided from time to time by the Board of Management (BOM) of the Institute, following guidelines issued by Ministry of Human Resource Development (MHRD), Government of India. The number of seats in each branch of the (M.TECH / M.B.A. / M.C.A.) programme will be decided by BOM as per the directives from Ministry of Human Resource Development (MHRD), Government of India and taking into account the market demands. Some seats for Non Resident Indians and a few seats for foreign nationals shall be made available.

2.2 The selected candidates will be admitted to the (M.TECH / M.B.A. / M.C.A.) programme after he/she fulfills all the admission requirements set by the Institute and after payment of the prescribed fees.

2.3 Candidates for admission to the first semester of the Master's Degree Programme shall be required to have passed an appropriate Degree Examination recognized by Hindustan University.

2.4 In all matters relating to admission to the (M.TECH / M.B.A. / M.C.A.). Programme, the decision of the Institute and its interpretation given by the Chancellor of the Institute shall be final.

2.5 If at any time after admission, it is found that a candidate has not fulfilled any of the requirements stipulated by the Institute, the Institute may revoke the admission of the candidate with information to the Academic Council.

3. Structure of the programme

3.1 The programme of instruction will have the following structure

i) Core courses of Engineering / Technology / Management.

ii) Elective courses for specialization in areas of student's choice

3.2 The minimum durations of the programmes are as given below:

Program	No. of Semesters
M.Tech.(Full-Time)	4
M.Tech.(Part -Time)	6
M.B.A. (Full - Time)	4
M.B.A. (Part - Time)	6
M.C.A.(Full - Time)	6
M.C.A.(Part -Time)	8

Every (M.TECH / M.B.A. / M.C.A.) programme will have a curriculum and syllabi for the courses approved by the Academic Council.

3.3 Each course is normally assigned certain number of credits. The following norms will generally be followed in assigning credits for courses.

- One credit for each lecture hour per week per semester
- One credit for each tutorial hour per week per semester
- One credit for each laboratory practical of three hours per week per semester.
- One credit for 4 weeks of industrial training and
- One credit for 2 hours of project per week per semester.

3.4 For the award of degree, a student has to earn certain minimum total number of credits specified in the curriculum of the relevant branch of study. The curriculum of the different programs shall be so designed that the minimum prescribed credits required for the award of the degree shall be within the limits specified below.

Program	Minimum prescribed credit range
M.Tech. (Full time / Part time)	75 - 85
M.B.A. (Full time / Part time)	85 - 95
M.C.A (Full time / Part time)	115 - 125

3.5 The medium of instruction, examination and the language of the project reports will be English.

4. Faculty Advisor

4.1 To help the students in planning their courses of study and for getting general advice on the academic programme, the concerned Department will assign a certain number of students to a Faculty member who will be called their Faculty Advisor.

5. Class Committee

5.1 A Class Committee consisting of the following will be constituted by the Head of the Department for each class:

(i) A Chairman, who is not teaching the class.

(ii) All subject teachers of the class.

(iii) Two students nominated by the department in consultation with the class.

The Class Committee will meet as often as necessary, but not less than three times during a semester.

The functions of the Class Committee will include:

(i) Addressing problems experienced by students in the classroom and the laboratories.

(ii) Analyzing the performance of the students of the class after each test and finding ways and means of addressing problems, if any.

(iii) During the meetings, the student members shall express the opinions and suggestions of the class students to improve the teaching / learning process.

6. Grading

6.1 A grading system as below will be adhered to.

Range of Marks	Letter Grade	Grade points
95-100	S	10
85 - 94	A	09
75- 84	B	08
65-74	C	07
55-64	D	06
50-54	E	05
< 50	U	00
	I (Incomplete)	–

6.2 GPA & CGPA

GPA is the ratio of the sum of the product of the number of credits C_i of course "i " and the grade points P_i earned for that course taken over all courses "i" registered by the student to the sum of Ci for all "i ". That is,

$$GPA = \frac{\sum_i C_i P_i}{\sum_i C_i}$$

CGPA will be calculated in a similar manner, at any semester, considering all the courses enrolled from first semester onwards.

6.3 For the students with letter grade I in certain subjects, the same will not be included in the computation of GPA and CGPA until after those grades are converted to the regular grades.

6.4 Raw marks will be moderated by a moderation board appointed by the Vice-Chancellor of the University. The final marks will be graded using an absolute grading system. The Constitution and composition of the moderation board will be dealt with separately.

7. Registration and Enrollment

7.1 Except for the first semester, registration and enrollment will be done in the beginning of the semester as per the schedule announced by the University.

7.2 A student will be eligible for enrollment only if he/she satisfies regulation 10 (maximum duration of the programme) and will be permitted to enroll if (i) he/she has cleared all dues in the Institute, Hostel & Library up to the end of the

previous semester and (ii) he/she is not debarred from enrollment by a disciplinary action of the University.

7.3 Students are required to submit registration form duly filled in.

8. Registration requirement

8.1 **(i)** A Full time student shall not register for less than 16 credits or more than 26 credits in any given semester.

8.1 **(ii)** A part time student shall not register for less than 10 credits or more than 20 credits in any given semester.

8.2 If a student finds his/her load heavy in any semester, or for any other valid reason, he/she may withdraw from the courses within three weeks of the commencement of the semester with the written approval of his/her Faculty Advisor and HOD. However the student should ensure that the total number of credits registered for in any semester should enable him/her to earn the minimum number of credits per semester for the completed semesters.

9. Minimum requirement to continue the programme

9.1 For those students who have not earned the minimum required credit prescribed for that particular semester examination, a warning letter to the concerned student and also to his parents regarding the shortage of his credit will be sent by the HOD after the announcement of the results of the university examinations.

10. Maximum duration of the programme

The minimum and maximum period for the completion of various programs are given below.

Program	Min. No. of Semesters	Max. No. of Semesters
M.Tech (Full - time)	4	8
M.Tech (Part - time)	6	10
M.B.A. (Full Time)	4	8
M.B.A. (Part Time)	6	10
M.C.A. (Full - Time)	6	12
M.C.A (Part -Time)	8	14

11. Temporary discontinuation

11.1 A student may be permitted by the Director(academic) to discontinue temporarily from the programme for a semester or a longer period for reasons of ill health or other valid reasons. Normally a student will be permitted to discontinue from the programme only for a maximum duration of two semesters.

12. Discipline

12.1 Every student is required to observe discipline and decorum both inside and outside the campus and not to indulge in any activity which will tend to bring down the prestige of the University.

12.2 Any act of indiscipline of a student reported to the Director (Academic) will be referred to a Discipline Committee so constituted. The Committee will enquire into the charges and decide on suitable punishment if the charges are substantiated. The committee will also authorize the Director(Academic) to recommend to the Vice-Chancellor the implementation of the decision. The student concerned may appeal to the Vice-Chancellor whose decision will be final. The Director (Academic) will report the action taken at the next meeting of the Council.

12.3 Ragging and harassment of women are strictly prohibited in the University campus and hostels.

13. Attendance

13.1 A student whose attendance is less than 75% is not eligible to appear for the end semester examination for that semester. The details of all students who have attendance less than 75% will be announced by the teacher in the class. These details will be sent to the concerned HODs and Director (Academic).

13.2 Those who have less than 75% attendance will be considered for condonation of shortage of attendance. However a condonation of 10% in attendance will be given on medical reasons. Application for condonation recommended by the Faculty Advisor, concerned faculty member and the HOD is to be submitted to the Director (Academic) who, depending on the merits of the case, may permit the student to appear for the end semester examination. A student will be eligible for this concession at most in two semesters during the entire degree programme. Application for medical leave, supported by medical certificate with endorsement by a Registered Medical Officer, should reach the HOD within seven days after returning from leave or, on or before the last instructional day of the semester, whichever is earlier.

13.3 As an incentive to those students who are involved in extra curricular activities such as representing the University in Sports and Games, Cultural Festivals, and Technical Festivals, NCC/ NSS events, a relaxation of up to 10% attendance will be given subject to the condition that these students take prior approval from the officer-in-charge. All such applications should be recommended by the concerned HOD and forwarded to Director (Academic) within seven instructional days after the programme/activity.

14. Assessment Procedure

14.1 The Academic Council will decide from time to time the system of tests and examinations in each subject in each semester.

14.2 For each theory course, the assessment will be done on a continuous basis as follows:

Test / Exam	Weightage	Duration of Test Exam
First Periodical Test*	10%	2 Periods
Second Periodical Test*	10%	2 Periods
Model exam	20%	3 hours
Seminar/ Assignments/Quiz	20%	
End - semester examination	50%	3 Hours

*** Best out of the two tests will be considered.**

14.3 For practical courses, the assessment will be done by the subject teachers as below:

(i) Weekly assignment/Observation note book / lab records - weightage 60%.

(ii) End semester examination of 3 hours duration including viva - weightage 40%

15. Make up Examination/model examination

15.1 Students who miss the end-semester examinations / model examination for valid reasons are eligible for make-up examination /model examination. Those

who miss the end-semester examination / model examination should apply to the Head of the Department concerned within five days after he / she missed examination, giving reasons for absence.

15.2 Permission to appear for make-up examination / model exam will be given under exceptional circumstances such as admission to a hospital due to illness. Students should produce a medical certificate issued by a Registered Medical Practitioner certifying that he/she was admitted to hospital during the period of examination / model exam and the same should be duly endorsed by parent / guardian and also by a medical officer of the University within 5 days.

16. Project evaluation

16.1 For Project work, the assessment will be done on a continuous basis as follows:

Review / Examination	Weightage
First Review	10%
Second Review	20%
Third Review	20%
End semester Examination	50%

For end semester exam, the student will submit a Project Report in a format specified by the Director (Academic). The first three reviews will be conducted by a Committee constituted by the Head of the Department. The end - semester examination will be conducted by a Committee constituted by the Controller of Examinations. This will include an external expert.

17. Declaration of results

17.1 A candidate who secures not less than 50% of total marks prescribed for a course with a minimum of 50% of the marks prescribed for the end semester examination shall be declared to have passed the course and earned the specified credits for the course.

17.2 After the valuation of the answer scripts, the tabulated results are to be scrutinized by the Result Passing Boards of PG programmes constituted by the Vice-Chancellor. The recommendations of the Result Passing Boards will be placed before the Standing Sub Committee of the Academic Council constituted by the Chancellor for scrutiny. The minutes of the Standing Sub Committee along with the results are to be placed before the Vice-Chancellor for approval. After getting the approval of the Vice-Chancellor, the results will be published by the Controller of Examination/ Registrar.

17.3 If a candidate fails to secure a pass in a course due to not satisfying the minimum requirement in the end semester examination, he/she shall register and re-appear for the end semester examination during the following semester. However, the sessional marks secured by the candidate will be retained for all such attempts.

17.4 If a candidate fails to secure a pass in a course due to insufficient sessional marks though meeting the minimum requirements of the end semester examination, wishes to improve on his/ her sessional marks, he/she will have to register for the particular course and

attend the course with permission of the HOD concerned and the Registrar. The sessional and external marks obtained by the candidate in this case will replace the earlier result.

17.5 A candidate can apply for the revaluation of his/her end semester examination answer paper in a theory course within 2 weeks from the declaration of the results, on payment of a prescribed fee through proper application to the Registrar/Controller of Examinations through the Head of the Department. The Registrar/ Controller of Examination will arrange for the revaluation and the results will be intimated to the candidate concerned through the Head of the Department. Revaluation is not permitted for practical courses and for project work.

17.6 The weightage for internal marks in finalizing results and grades shall be waived off after completion of 5 semesters.

18. Grade Card

18.1 After results are declared, grade sheet will be issued to each student, which will contain the following details:

(i) Program and branch for which the student has enrolled.

(ii) Semester of registration.

(iii) List of courses registered during the semester and the grade scored.

(iv) Semester Grade Point Average (GPA)

(v) Cumulative Grade Point Average (CGPA).

19. Class / Division

19.1 Classification is based on CGPA and is as follows:

CGPA $\geq$ 8.0 : **First Class with distinction**

$6.5 \leq$ CGPA < 8.0 : **First Class**

$5.0 \leq$ CGPA < 6.5 : **Second Class.**

19.2 (i) Further, the award of 'First class with distinction' is subject to the candidate becoming eligible for the award of the degree having passed the examination in all the courses in his/her first appearance within the minimum duration of the programme.

(ii) The award of 'First Class' is further subject to the candidate becoming eligible to the award of the degree having passed the examination in all the courses within the below mentioned duration of the programme.

Program	No. of Semesters
M.Tech.(Full-Time)	5
M.Tech.(Part -Time)	7
M.B.A. (Full - Time)	5
M.B.A. (Part - Time)	7
M.C.A.(Full - Time)	7
M.C.A.(Part -Time)	9

(iii) The period of authorized discontinuation of the programme (vide clause 11.1) will not be counted for the purpose of the above classification.

20. Transfer of credits

20.1 Within the broad framework of these regulations, the Academic Council, based on the recommendation of the transfer of credits committee so constituted by the Chancellor may permit students to earn part of the credit requirement in other approved institutions of repute and status in the country or abroad.

21. Eligibility for the award of (M.TECH / M.B.A. / M.C.A.) Degree

21.1 A student will be declared to be eligible for the award of the (M.TECH / M.B.A. / M.C.A.). Degree if he/she has

i) registered and successfully credited all the core courses,

ii) successfully acquired the credits in the different categories as specified in the curriculum corresponding to the discipline (branch) of his/her study within the stipulated time,

iii) has no dues to all sections of the Institute including Hostels, and

iv) has no disciplinary action pending against him/her.

The award of the degree must be recommended by the Academic Council and approved by the Board of Management of the University.

22. Power to modify

22.1 Notwithstanding all that has been stated above, the Academic Council has the right to modify any of the above regulations from time to time subject to approval by the Board of Management.

HINDUSTAN UNIVERSITY

HHINDUSTAN INSTITUTE OF TECHNOLOGY AND SCIENCE

DEPARTMENT OF ELECTRICAL AND ELECTRONICS ENGINEERING

M.Tech. (Applied Electronics)

CURRICULUM 2013

Objective of the programme

To provide the students with an insight into the theoretical and application aspects of advanced digital system design, signal processing, VLSI, microprocessors and microcontrollers, communication networks, EMI/EMC, ASIC design etc., to enable them to pursue further academic work or research and development in this field.

SEMESTER I

Sl. No.	Course Code	Course Title	L	T	P	C	TCH
Theory							
1	PMA106	Advanced Applied Mathematics *	3	1	0	4	4
2	PCS101	Advanced Digital Signal Processing$	3	1	0	4	4
3	PAL101	Advanced Digital System Design**	3	1	0	4	4
4	PVL102	Digital CMOS design+	3	1	0	4	4
5	PES102	Embedded System Design**	3	1	0	4	4
6	PES103	Advanced Microprocessors**	3	1	0	4	4
Practicals							
7	PAL102	Electronics Design Lab I	0	0	3	2	3
		Total				**26**	**27**

*** Common to MTECH (CS)/ MTECH (PC&I)/ MTECH (C&CE)/ MTECH (ES)/MTECH(VLSI)**

$ Common to MTECH(CCE) and M.TECH(CS)

****Common to M.TECH(ES)**

+ Common to MTECH(VLSI)

SEMESTER II

Sl. No.	Course Code	Course Title	L	T	P	C	TCH
Theory							
1	PAL201	Analysis and Design of Analog Integrated Circuits	3	1	0	4	4
2	PAL202	Computer Architecture and Parallel Processing	3	1	0	4	4
3	PAL203	Digital Control Engineering	3	1	0	4	4
4	PAL204	High Performance Communication Networks	3	1	0	4	4
5	-	Elective I	3	1	0	4	4
6	-	Elective II	3	1	0	4	4
Practical							
7	PAL205	Electronic Design Lab II	0	0	3	2	3
		Total				**26**	**27**

SEMESTER III

Sl. No.	Course Code	Course Title	L	T	P	C	TCH
Theory							
1	-	Elective III	3	1	0	4	4
2	-	Elective IV	3	1	0	4	4
3	-	Elective V	3	1	0	4	4
Practical							
4	PAL301	Project Work (Phase I)	0	0	12	6	12
		Total				**18**	**24**

SEMESTER IV

Sl. No.	Course Code	Course Title	L	T	P	C	TCH
Theory							
1	PAL401	Project Work (Phase II)	0	0	24	12	24
		Total				**12**	**24**

TOTAL CREDITS-82

ELECTIVE COURSES

Sl.No	Course Code	Course Title	L	T	P	C	TCH
1	PAL701	Neural Networks and Applications	3	1	0	4	4
2	PAL702	Robotics	3	1	0	4	4
3	PAL703	ASIC Design	3	1	0	4	4
4	PCS708	Electromagnetic Interference and Compatibility in System Design**	3	1	0	4	4
5	PVL703	Low Power VLSI Design	3	1	0	4	4
6	PAL704	Digital Signal Processors$	3	1	0	4	4
7	PCS706	Digital Image Processing*	3	1	0	4	4

*** Common to M.TECH. (CS) ** Common to M.TECH. (CS)/M.TECH.(EC)**

$ Common to M.TECH(PED)

HINDUSTAN UNIVERSITY
HINDUSTAN INSTITUTE OF TECHNOLOGY AND SCIENCE

DEPARTMENT OF ELECTRICAL AND ELECTRONICS ENGINEERING
(M.Tech. Applied Electronics)

CURRICULUM 2013

PMA106 ADVANCED APPLIED MATHEMATICS

Common to MTECH (CS)/ MTECH (PC&I)/ MTECH (C&CE)/ MTECH (ES)/MTECH(VLSI)

L	T	P	C
3	1	0	4

Goal

Develop the Mathematical skills to formulate certain practical problems, solve them and physically interpret the results

Objectives

The course should enable the student to

1. Understand the techniques to solve the system of equations using direct method and indirect methods. Learns to decompose the matrix in the LU form and to find the Eigen value of a matrix using power and Jacobi methods.
2. Learn to classify the initial and boundary value problems. Understands the D'Alemberts solution of the one dimensional wave equation. Learn significance of characteristic curves.
3. Learn series solutions of Bessel's and Legendre equations. Understand recurrence relation, generating functions and orthogonal properties.
4. Learn basics of probability, addition and multiplication, Baye's theorems. Understands the concept of random variable, moment generating function and their properties. Learn standard distributions in discrete and continuous cases
5. Learns the different Markovian models with finite and infinite capacity and understands to classify them.

Outcome

The students should be able to:

1. Write the algorithm for solving the simultaneous equations for direct and indirect methods. Identifies the Eigen values using conventional method and compares with numerical solutions. He should be able to write the algorithm to find the Eigen values of a matrix.
2. Form the wave equations with initial conditions and solve them using D'Alemberts solutions. Solve the wave equations using Laplace transform for displacements in long string - long string under its weight and free and forced vibrations.
3. Solve the Bessel's equation and Legendre equations. To solve many practical problems that arise in electrical transmission problems and vibration of membranes as in loudspeakers using bessels function.

4. Evaluates the probability using addition and multiplication theorem. Applies Baye's for practical problems to find the probability. Verifies whether a given function is a probability mass or density function. Applies the discrete and continuous distributions for solving practical problems. Evaluate the moments of the distributions using moment generating function.

5. Analyze and classify the models, M / M / 1, M / M / C, finite and infinite capacity and solve practical problems related to the queuing models.

UNIT I LINEAR ALGEBRAIC EQUATION AND EIGEN VALUE PROBLEMS 12

System of Equations - Solution by Gauss Elimination and Gauss Jordan methods - LU decomposition method - Indirect methods - Gauss Jacobi and Gauss Seidel methods - Eigen values of a matrix using Jacobi and power methods.

UNIT II WAVE EQUATION 12

Solution of initial and boundary value problems - Characteristics - D'Alembert's solution - Significance of characteristic curves - Laplace transform solutions for displacement in a long string, in a long string under its weight - a bar with prescribed force on one end - Free vibrations of a string.

UNIT III SPECIAL FUNCTIONS 12

Series solutions - Bessel's equation - Bessel functions - Legendre's equation - Legendre polynomials - Rodrigue's formula - Recurrence relations - Generating functions and orthogonal property for Bessel functions of the first kind - Legendre polynomials.

UNIT IV PROBABILITY AND RANDOM VARIABLE 12

Discrete and Continuous random variables - Moments - Moment generating functions - Standard distributions - Binomial, Poisson, Geometric, Negative Binomial, Uniform, Normal ,Exponential, Gamma and Weibull distributions - Two dimensional random variables - Joint, Marginal and Conditional distributions. Correlation and Regression.

UNIT V QUEUING THEORY 12

Markovian models - Birth and death queuing models - Steady state - Single and Multiple servers - M/M/1 - Finite and infinite capacity - M/M/C - finite and infinite capacity.

L = 45 T = 15 TOTAL = 60

REFERENCES

1) Taha, H.A., "Operations Research - An Introduction ", Prentice Hall of India Ltd., 6th Edition, New Delhi, 1997.

2) Dr.Singaravelu A., Dr.Siva Subramanian S., and Dr.Ramachandran C., "Probability and Queuing Theory", Meenakshi agency, 20th edition, January 2013.

3) Veerarajan T., "Probability, Statistics and Random Processes", Tata McGraw-Hill, second edition, 2004.

4) Grewal B.S., "Higher Engineering Mathematics", Khanna Publishers, 34th edition.

5) Sankara Rao K., "Introduction to Partial Differential Equations", PHI, 1995.

6) Veerarajan T., "Mathematics IV", Tata McGraw-Hill, 2000.

PCS101 ADVANCED DIGITAL SIGNAL PROCESSING
Common to MTECH(CCE) and M.TECH(CS)

L	T	P	C
3	1	0	4

Prerequisite

Basic knowledge of random processes, Fourier Transform, auto-correlation matrices & sampling process.

Goal

To provide knowledge of digital signal processing methods and tools, including leading algorithms for various applications.

Objectives

The course will enable the students to:

(i) Know the basics of discrete random processes

(ii) Know the basics of various Spectrum estimation methods

(iii) Know the basics of linear estimators & predictors

(iv) Know the basics of various adaptive filters along with their applications

(v) Know the fundamentals of multirate digital signal processing

Outcome

At the end of the course the students should be able to

(i) Understand the various theorems & processing that are done on discrete random processes

(ii) Understand the different parametric & non-parametric spectrum estimation methods

(iii) Understand the linear predictors & Wiener filters

(iv) Understand the adaptive filters & their various applications

(v) Understand the importance of multirate digital signal processing

UNIT I DISCRETE RANDOM SIGNAL PROCESSING **9**

Discrete Random Processes- Ensemble averages, stationary processes, Autocorrelation and Auto covariance matrices. Parseval's Theorem, Wiener-Khintchine Relation- Power Spectral Density- Periodogram Spectral Factorization, Filtering random processes. Low Pass Filtering of White Noise. Parameter estimation: Bias and consistency.

UNIT II SPECTRUM ESTIMATION **9**

Estimation of spectra from finite duration signals, Non-Parametric Methods-Correlation Method , Periodogram Estimator, Performance Analysis of Estimators -Unbiased, Consistent Estimators- Modified periodogram, Bartlett and Welch methods, Blackman -Tukey method. Parametric Methods

- AR, MA, ARMA model based spectral estimation. Parameter Estimation -Yule-Walker equations, solutions using Durbin's algorithm

UNIT III LINEAR ESTIMATION AND PREDICTION 9

Linear prediction- Forward and backward predictions, Solutions of the Normal equations- Levinson-Durbin algorithms. Least mean squared error criterion -Wiener filter for filtering and prediction , FIR Wiener filter and Wiener IIR filters ,Discrete Kalman filter

UNIT IV ADAPTIVE FILTERS 9

FIR adaptive filters -adaptive filter based on steepest descent method-Widrow-Hoff LMS adaptive algorithm, Normalized LMS. Adaptive channel equalization-Adaptive echo cancellation-Adaptive noise cancellation- Adaptive recursive filters (IIR). RLS adaptive filters-Exponentially weighted RLS-sliding window RLS.

UNIT V MULTIRATE DIGITAL SIGNAL PROCESSING 9

Mathematical description of change of sampling rate - Interpolation and Decimation , Decimation by an integer factor - Interpolation by an integer factor, Sampling rate conversion by a rational factor, Filter implementation for sampling rate conversion- direct form FIR structures, Polyphase filter structures, time-variant structures. Multistage implementation of multirate system. Application to sub band coding - Wavelet transform and filter bank implementation of wavelet expansion of signals.

L=45 T=15 Total=60

TEXT BOOK:

1. Monson H.Hayes, Statistical Digital Signal Processing and Modeling, John Wiley and Sons, Inc., Singapore, 2002.

REFERENCES:

1. John G. Proakis, Dimitris G.Manolakis, Digital Signal Processing Pearson Education, 2002.
2. John G. Proakis et.al.'Algorithms for Statistical Signal Processing', Pearson Education, 2002.
3. Dimitris G.Manolakis et.al.' Statistical and adaptive signal Processing', McGraw Hill, Newyork, 2000.
4. Rafael C. Gonzalez, Richard E.Woods, 'Digital Image Processing', Pearson Education, Inc., Second Edition, 2004.(For Wavelet Transform Topic)

PAL101 ADVANCED DIGITAL SYSTEM DESIGN
Common to M.TECH(ES)

L	T	P	C
3	1	0	4

Goal

To acquaint the students with the advanced topics in the digital systems analysis and design.

Objectives

The course will enable the students to:

(i) study the analysis and design of various types of CSSN, iterative networks and design using ASM charts.

(ii) understand the analysis and design of various types of asynchronous circuits and how to eliminate races and hazards

(iii) know various types of faults that can occur during fabrication , the methods for fault detection and faults in PLA.

(iv) give an insight into programmable logic devices and FPGA.

(v) study the VHDL code and use it for the design of logic devices

Outcome

After completion of the course, the students are expected to:

(i) gain the knowledge for designing different types of synchronous sequential circuits and use of ASM charts..

(ii) familiarize with the design ASCs and the problems involved in the design process and how to design circuits without hazards and races

(iii) know the types of faults in digital circuits, how to detect these faults , PLA minimization and fault diagnosis.

(iv) able to design CSSN using programmable logic devices and FPGA.

(v) learn VHDL and will be able to design various logic devices using VHDL

UNIT I SEQUENTIAL CIRCUIT DESIGN 9

Analysis of Clocked Synchronous Sequential Networks (CSSN) Modeling of CSSN - State table Reduction, State Assignment - Design of CSSN - Design of Iterative Circuits - ASM Chart.

UNIT II ASYNCHRONOUS SEQUENTIAL CIRCUIT DESIGN 9

Analysis of Asynchronous Sequential Circuit (ASC) - Flow Table Reduction - Races in ASC - State Assignment - Problem and the Transition Table - Design of ASC - Static and Dynamic Hazards - Essential Hazards - Data Synchronizers - Mixed Operating Mode Asynchronous Circuits.

UNIT III FAULT DIAGNOSIS AND TESTABILITY ALGORITHMS 9

Fault Table Method - Path Sensitization Method - Boolean Difference Method - Kohavi Algorithm - Tolerance Techniques - The Compact Algorithm - Practical PLA's - Fault in PLA - Test Generation - Masking Cycle - DFT Schemes - Built-in Self Test.

UNIT IV DESIGN OF CSSN USING PROGRAMMABLE DEVICES 9

EPROM to Realize a Sequential circuit. Programmable Logic Devices - Designing a Synchronous Sequential Circuit using a GAL- Realization State machine using PLD ,FPGA - Xilinx FPGA - Xilinx 2000 - Xilinx 3000

UNIT V SYSTEM DESIGN USING VHDL 9

VHDL Description of Combinational Circuits - Arrays - VHDL Operators - Compilation and Simulation of VHDL Code - Modeling using VHDL - Flip Flops - Registers - Counters - Sequential Machine -

Combinational Logic Circuits - VHDL Code for Serial Adder, Binary Multiplier , Binary Divider, complete Sequential Systems.

L =45 T=15 Total = 60

REFERENCES:

1. Donald G. Givone "Digital principles and Design" Tata McGraw Hill 2002.
2. John M Yarbrough "Digital Logic applications and Design" Thomson Learning, 2001
3. Nripendra N Biswas "Logic Design Theory" Prentice Hall of India, 2001
4. Charles H. Roth Jr. "Digital System Design using VHDL" Thomson Learning, 1998.
5. Charles H. Roth Jr. "Fundamentals of Logic design" Thomson Learning, 2004.
6. Stephen Brown and Zvonk Vranesic "Fundamentals of Digital Logic with VHDL Design" Tata McGraw Hill, 2002.
7. Navabi.Z. "VHDL Analysis and Modeling of Digital Systems. McGraw International, 1998
8. Parag K Lala, "Digital System design using PLD" BS Publications, 2003
9. Peter J Ashendem, "The Designers Guide to VHDL" Harcourt India Pvt Ltd, 2002
10. Mark Zwolinski, "Digital System Design with VHDL" Pearson Education, 2004
11. Skahill. K, "VHDL for Programmable Logic" Pearson education, 1996

PVL102 DIGITAL CMOS DESIGN
Common to MTECH(VLSI)

L	T	P	C
3	1	0	4

Goal

To provide knowledge about the basics of Digital CMOS design and the techniques available in it.

Objectives

The course will enable the students to:

(i) understand the theory, working and fabrication of different types of MOS transistors with current equation.

(ii) familiar with constructing inverters, stick diagrams and the design of combinational circuits

(iii) get exposed to sequential logic circuits design

(iv) familiarize with design of Arithmetic building blocks

(v) understand Verilog HDL programming and system Design

Outcome

After completion of the course the students are expected to be able to:

(i) Explain the theory and working of different types of MOS transistors, fabrication and design

equations

(ii) Construct inverters and other basic combinational circuits.

(iii) Build sequential logic circuits

(iv) Design Arithmetic building blocks.

(v) Gaining Verilog HDL programming skill and write test benches and programs for system design.

UNIT I MOS TRANSISTOR THEORY AND PROCESS TECHNOLOGY 9

NMOS and PMOS transistors, threshold voltage -body effect- design equations - second order effects,MOS models and small signal AC characteristics-Basic CMOS technology

UNIT II CMOS INVERTER AND COMBINATIONAL LOGIC 9

N MOS and C MOS inverters , stick diagram, propagation delay, Examples of combinational logic design, pass transistor logic - power dissipation

UNIT III SEQUENTIAL LOGIC CIRCUITS 9

Static and Dynamic Latches and Registers, Timing Issues, Pipelines, Clocking strategies, Synchronous and Asynchronous Design.

UNIT IV DESIGNING ARITHMETIC BUILDING BLOCKS 9

Datapath circuits, Architectures for Adders, Accumulators, Multipliers, Barrel Shifters, Memory Architectures, and Memory control circuits

UNIT V VERILOG HARDWARE DESCRIPTION LANGUAGE 9

Overview of digital design with Verilog HDL, hierarchical modeling concepts, modules and port definitions, gate level modeling, data flow modeling, behavioral modeling, task & functions, Test Bench.

L = 45 T = 15 Total = 60

REFERENCES

1. Jan Rabaey, Anantha Chandrakasan, B Nikolic, " Digital Integrated Circuits: A Design Perspective". Second Edition, Feb 2003, Prentice Hall of India.
2. N.Weste, K. Eshraghian, " Principles of CMOS VLSI Design". Second Edition, 1993 Addision Wesley,
3. M J Smith, "Application Specific Integrated Circuits", Addisson Wesley, 1997
4. Samir Palnitkar, "Verilog HDL", Pearson Education, 2nd Edition, 2004.
5. Eugene D.Fabricius, "Introduction to VLSI Design", McGraw Hill International Editions, 1990.
6. Pucknell, "Basic VLSI Design", Prentice Hall of India Publication, 1995.

PES102 EMBEDDED SYSTEN DESIGN
Common to M.TECH(ES)

L	T	P	C
3	1	0	4

Prerequisite Nil

Goal

The aim of this course is to expose the concepts of Embedded system principles and software development tools and to introduced PIC and Motorola microcontrollers and interfacing.

Objectives

The course should enable the students to:

(i) Understand the use of review in Embedded hardware,

(ii) Understand basic concepts of design of Embedded software system,

(iii) Understand the Software architecture and Developments tools

(iv) Understand the Operation of PIC microcontroller and interfacing

(v) Understand the Operation of Embedded Microcomputer systems

Outcome

At the end of the course the student should be able to:

(i) Use of hardware fundamentals.Gates.timing diagram,DMA,interrupts,built ins on the microprocessor and microprocessor architecture,

(ii) Explain the concept of Tasks,States,Data,Semaphores,more operating system servicesIR in RTOS environment,Basic design using RTOS,

(iii) Develop thorough basic knowledge on the behavior and the characteristics of Round-Robin techniques,Functions,Queue,Host and Target machine and Debugging techniques,

(iv) Learn the usage of Architecture,instruction sets of PIC, Loop time subroutine,I/O port expansion,I2C for peripherals chip access,ADC and UART special features,

(v) Acquire knowledge on the configuration of Motorolla,Registers,addressing modes,interfacing methods,ISR,Timing generations and measurements.

UNIT I INTRODUCTION : REVIEW OF EMBEDDED HARDWARE 9

Hardware Fundamentals: Terminology- Gates- Timing Diagram- Microprocessors- Buses- Direct Memory Access- Interrupts- Other Common Parts- Built-Ins on the Microprocessor-Conventions Used on Schematics. Interrupts: Microprocessor Architecture - Interrupts Basics-Shared-Data Problem- Interrupt Latency, Examples of Embedded System.

UNIT II DESIGN OF EMBEDDED SOFTWARE SYSTEM 9

Introduction: Tasks and Task States- Tasks and Data- Semaphores and Shared Data. More Operating System Services: Message Queues- Mailboxes and Pipes- Timer Functions- Events- Memory Management- Interrupt Routines in an RTOS Environment, Basic Design Using a Real-Time Operating

System.

UNIT III SOFTWARE ARCHITECTURES AND DEVELOPMENT AND TOOLS

Software Architectures: Round-Robin- Round-Robin with Interrupts- Function-Queue- Scheduling Architecture- Real-Time Operating System Architecture, Development Tools: Host and Target Machines- Linker/Locators for Embedded Software, Debugging Techniques.

UNIT IV PIC MICROCONTROLLER AND INTERFACING 9

Introduction- CPU Architecture and Instruction Set- Loop Time Subroutine- Timer2 and Interrupts- Interrupts Timing- I/O Port Expansion- I2C Bus for Peripheral Chip Access- Analog-to- Digital Converter- UART- Special Features.

UNIT V EMBEDDED MICROCOMPUTER SYSTEMS 9

Motorola MC68H11 Family Architecture - Registers- Addressing Modes. Interfacing Methods: Parallel I/O Interface- Parallel Port Interfaces- Memory Interfacing- High Speed I/O interfacing-Analog interfacing, Interrupts, Interrupt Service Routine- Features of Interrupts- Interrupt Vector and Priority, Timing Generation and Measurements: Input Capture- Output Compare- Frequency Measurement, Serial I/O Devices: RS232- RS485.

L = 45, T = 15, TOTAL= 60

TEXT BOOKS

1. David E Simon, An Embedded Software Primer, Pearson Education Asia, 2001
2. John B. Peat man , Design with Microcontroller, Pearson Education Asia, 1998
3. Jonarthan W. Valvano Brooks/cole, Embedded Micro Computer Systems, Real Time Interfacing, Thomson Learning 2001

REFERENCES

1. Burns, Alan and Wellings, Andy, Real-Time Systems and Programming Languages, Second Edition, Harlow: Addison-Wesley-Longman, 1997
2. Raymond J.A. Bhur and Donald L.Bialey, An Introduction to Real Time Systems: Design to Networking with C/C++, Prentice Hall Inc, NewJersey, 1999
3. Grehan Moore, and Cyliax, Real Time Programming: A Guide to 32 Bit Embedded Development. Reading: Addison-Wesley-Longman, 1998
4. Heath, Steve, Embedded Systems Design. Newnes , 1997PES103 ADVANCED MICRO PROCESSORS

PES103 ADVANCED MICROPROCESSORS
COMMON TO M.TECH(ES)

L	T	P	C
3	1	0	4

Prerequisite Nil

Goal

The aim of this course is to give an in depth knowledge on Advanced Microprocessor

Objectives

The course should enable the students to:

1. Understand the use of 16/32 bit Microprocessor
2. Understand about Assembly level programming
3. Understand the Operation of Digital interfacing
4. Understand the Operation Multiprocessor configuration and introduction to Microprogrammable microprocessors
5. Learn about High performance RISC Architecture.

Outcomes

At the end of the course the student should be able to:

1. Gain basics of Organization of 8086,80286,80386,80486, Minimum maximum mode, pipeline architecture, addressing modes, memory registration, segmentation, Bus structure and timing, expectation handling,
2. Explain the concept of Assembly level programming of 8086, Instruction types, Macros and Byte string manipulation
3. Develop through basic knowledge on the behavior and the characteristics Programming parallel ports, Keypad interfacing alphaneumeric display, interfacing high power devices, optical motor shaft encoder, sensor and transducers, convertors and 8086 based control systems
4. Learn the usage of Queue status and lock facility,8086/8088 based multiprocessing system, 8087 NDP, 8089, Pentium 4 processor, organization of bit slice processor for microprogrammed machines,
5. Acquire knowledge on the configuration of ARM 7 Organization and implementation, instruction sets, Basic ARM 7 ALP, ARM CPU cores.

UNIT I 16/ 32 BIT MICROPROCESSOR 9

Organization of 8086, 80286,80386,80486 microprocessors - Minimum maximum mode - Pipeline Architecture - Registers - Addressing modes - Memory Registration - Memory Segmentation - Instruction set of 8086 - Bus structure and timing - exception handling.

UNIT II ASSEMBLY LANGUAGE PROGRAMMING 9

Assembly language programming of 8086 microprocessor - Data transfer instruction - Arithmetic

instruction - Branch instructions - Loop instructions - NOP and HALT instructions - Flag manipulation instructions - Logical instructions - Shift and rotate instructions - linking and relocation - stacks procedure - Interrupts and interrupt routines - Macros - Byte and string manipulations.

UNIT III DIGITAL INTERFACING **9**

Programming Parallel ports - Handshake input/output - interfacing a microprocessor to a keyboard, interfacing to alphanumeric displays, interfacing a microcomputer to high power devices, Optical motor shaft encoders - Sensors and Transducers - D/A converter operations, interfacing & applications- A/D converter Specifications, types & interfacing, A 8086 based process control system.

UNIT IV MULTIPROCESSOR CONFIGURATIONS, ADVANCED MICROPROCESSOR ARCHITECTURE, INTRODUCTION TO THE MICROPROGRAMMABLE MICROPROCESSORS **9**

Queue status and lock facilities - 8086 / 8088 based multiprocessing system, 8087 numeric data processor, 8089 I/O processor. Introduction to Motorola 68HC11 processor, Pentium4 Microprocessor, Architecture, Instruction set and addressing modes, Organization of bit-slice processor, bit-slice processor architecture for micro-programmed machines.

UNIT V HIGH PERFORMANCE RISC ARCHITECTURE **9**

ARM: The ARM7 architecture - ARM7 organization and implementation - The ARM7 instruction set - The thumb instruction set - Basic ARM7 Assembly language program - ARM CPU cores.

L = 45, T = 15, TOTAL = 60

TEXT BOOKS:

1. Barry B. Brey, "The Intel Microprocessors Architecture, Programming and Interfacing", PHI, 2002 (UNIT I,II,III)
2. Hall.D.V, "Microprocessor and Interfacing: Programming and hardware", McGraw Hill Book Company, New York, 1988 (UNIT III)
3. Liu.Y and Gibson. G. A., "Microcomputer systems: The 8086/ 8088 family: Architecture, Programming and design", Prentice Hall of India Pvt. Ltd, M.D. (1979) (UNIT IV).
4. John Mick and Jim Brick, "Bit-slice Microprocessor Design", McGraw-Hill, 1980 (UNIT IV).
5. Steave Furber, "ARM system - on - chip architecture", Addison Wesley, 2000. (UNIT V)

REFERENCES:

1. Daniel Tabak, "Advanced Microprocessors", McGraw Hill. Inc., 1995
2. James L. Antonakos, "The Pentium Microprocessor", Pearson Education, 1997
3. James L Antonakos, "An Introduction to the Intel family of Microprocessors", Pearson Education, 1999

PAL102 ELECTRONICS DESIGN LABORATORY I

L	T	P	C
0	0	3	2

Goal

To give hands on experience about Micro Controller, VHDL programming and DSP processor.

Objectives

The course will enable the students to:

(i) Know the designing of PIC microcontroller & 16-bit microcontroller

(ii) Know the designing of ALU using FPGA.

(iii) Know the modeling of Sequential digital systems using VHDL & verilog.

(iv) Know the implementation of adaptive filters, periodogram & QMF in DSP processor

(v) Know the simulation of NMOS & CMOS circuits

Outcome

At the end of the course the students should be able to

(i) Design system using PIC microcontroller & 16-bit microprocessor

(ii) Design ALU operations using FPGA packages

(iii) Simulate & model sequential digital circuits like flip-flops using VHDL & verilog HDL.

(iv) Implement digital signal processors like-adaptive filters, periodogram, QMF in DSP processors using MATLAB.

(v) Simulate NMOS & CMOS circuits using SPICE software.

List of Experiments:

1. System design using PIC Microcontroller.
2. Implementation of Adaptive Filters, periodogram and multistage multirate system in DSP Processor
3. Simulation of QMF using Simulation Packages
4. Modeling of Sequential Digital system using VHDL.
5. Modeling of Sequential Digital system using Verilog.
6. Design and Implementation of ALU using FPGA.
7. Simulation of NMOS and CMOS circuits using SPICE.
8. System design using 16- bit Microprocessor.

Total = 45

SEMESTER II

PAL201 ANALYSIS AND DESIGN OF ANALOG INTEGRATED CIRCUITS

L	T	P	C
3	1	0	4

Goal

To analyze and design bipolar and MOS types of IC circuits..

Objectives

The course will enable the students to:

(i) Understand the concept of integrated active devices and their models.

(ii) Know the types of current sources , their applications and output stages used for IC devices

(iii) Have an insight into the internal structure , operation and characteristics of IC 741 OPAMP.

(iv) Get knowledge of various modes of operation of analog multiplier and PLL.

(v) Acquire knowledge in MOS analog devices

Outcome

After completion of the course, the students are expected to:

(i) Get familiarize with the bipolar and MOS active IC devices and their large and small signal models .

(ii) Get an insight into the types of current sources and output stages.

(iii) Understand the internal structure , operation and characteristics of IC 741 OPAMP.

(iv) Get a clear idea of multiplier applications and PLL ICs.

(v) Gain information about MOS IC devices and their benefits

UNIT I MODELS FOR INTEGRATED CIRCUIT ACTIVE DEVICES 9

Depletion region of a PN junction - large signal behavior of bipolar transistors- small signal model of bipolar transistor- large signal behavior of MOSFET- small signal model of the MOS transistors- short channel effects in MOS transistors - weak inversion in MOS transistors- substrate current flow in MOS transistor.

UNIT II CIRCUIT CONFIGURATION FOR LINEAR IC 9

Current sources, Analysis of difference amplifiers with active load using BJT and FET, supply and temperature independent biasing techniques, voltage references. Output stages: Emitter follower, source follower and Push pull output stages.

UNIT III OPERATIONAL AMPLIFIERS 9

Analysis of operational amplifiers circuit, slew rate model and high frequency analysis, Frequency response of integrated circuits: Single stage and multistage amplifiers, Operational amplifier noise

UNIT IV ANALOG MULTIPLIER AND PLL **9**

Analysis of four quadrant and variable trans conductance multiplier, voltage controlled oscillator, closed loop analysis of PLL, Monolithic PLL design in integrated circuits: Sources of noise- Noise models of Integrated-circuit Components - Circuit Noise Calculations - Equivalent Input Noise Generators - Noise Bandwidth - Noise Figure and Noise Temperature

UNIT V ANALOG DESIGN WITH MOS TECHNOLOGY **9**

MOS Current Mirrors - Simple, Cascode, Wilson and Widlar current source - CMOS Class AB output stages - Two stage MOS Operational Amplifiers, with Cascode, MOS Telescopic-Cascode Operational Amplifier - MOS Folded Cascode and MOS Active Cascode Operational Amplifiers

L=45, T=15,Total=60

REFERENCES

1. Gray, Meyer, Lewis, Hurst, "Analysis and design of Analog IC's", Fourth Edition, Willey International, 2002.
2. Behzad Razavi, "Principles of data conversion system design", S.Chand and company ltd, 2000
3. Nandita Dasgupata, Amitava Dasgupta,"Semiconductor Devices, Modelling and Technology", Prentice Hall of India pvt. ltd, 2004.
4. Grebene, Bipolar and MOS Analog Integrated circuit design", John Wiley & sons,Inc.,2003.
5. Phillip E.Allen Douglas R. Holberg, "CMOS Analog Circuit Design", Second Edition-Oxford University Press-2003

PAL202 COMPUTER ARCHITECTURE AND PARALLEL PROCESSING

L	T	P	C
3	1	0	4

Goal

To introduce the principles of hardware and software parallelism and computer architecture.

Objectives

The course should enable the students :

(i) To impart knowledge on different models of parallel computers conditions and machines of parallel processing.

(ii) The objectives of this unit is to impart knowledge in the processor technology, types of processors memory hierarchy technology.

(iii) To impart knowledge on pipelining.

(iv) To impart knowledge in multithreading, dataflow architecture.

(v) To learn about languages.

Outcome

At the end of the course the student should be able to:

(i) do parallel models both hardware and software.

(ii) analysis to choose the processors memory according to the applications.

(iii) explain about pipelining message passing architecture.

(iv) know the design of multithreading principles and rules.

UNIT I PRINCIPLES OF PARALLEL PROCESSING 9

Multiprocessors and Multicomputers - Multivector and SIMD Computers- PRAM and VLSI Models- Conditions of Parallelism- Program Partitioning and scheduling-program flow mechanisms- parallel processing applications- speed up performance law.

UNIT II PROCESSOR AND MEMORY ORGANIZATION 9

Advanced processor technology - Superscalar and vector processors- Memory hierarchy technology- Virtual memory technology- Cache memory organization- Shared memory organization.

UNIT III PIPELINE AND PARALLEL ARCHITECTURE 9

Linear pipeline processors- Non linear pipeline processors- Instruction pipeline design- Arithmetic design- Superscalar and super pipeline design- Multiprocessor system interconnects- Message passing mechanisms.

UNIT IV VECTOR, MULTITHREAD AND DATAFLOW ARCHITECTURE 9

Vector Processing principle- Multivector Multiprocessors- Compound Vector processing- Principles of multithreading-fine grain multicomputers- scalable and multithread architectures - Dataflow and hybrid architectures.

UNIT V SOFTWARE AND PARALLEL PROCESSING 9

Parallel programming models- parallel languages and compilers- parallel programming environments- synchronization and multiprocessing modes- message passing program development- mapping programs onto multicomputers- multiprocessor UNIX design goals- MACH/OS kernel architecture- OSF/1 architecture and applications.

L=45, T=15,Total=60

REFERENCES

1. Kai Hwang, "Advanced Computer Architecture", TMH 2001.
2. William Stallings, Computer Organization and Architecture, McMillan Publishing Company, 1990.
3. M.J. Quinn, "Designing efficient Algorithms for parallel computer", McGraw Hill International, 1994.

PAL203 DIGITAL CONTROL ENGINEERING

L	T	P	C
3	1	0	4

Prerequisite CONTROL SYSTEMS

Goal

To expose the student the analysis and design of digital control systems.

Objectives

The course should enable the students to:

(i) Acquaint the student with the fundamentals of control theory

(ii) Know about the signal processing in digital control systems

(iii) Study the modeling and analysis of sampled data control systems

(iv) Design control algorithms to confine system behavior to designated specifications

(v) Understand the practical aspects of digital control algorithms

Outcome

At the end of the course the student should be able to:

(i) Familiarize the fundamental concepts of continuous control systems.

(ii) Understand the sampled-data systems & mathematical representation of analog to digital & digital to analog conversions.

(iii) Understand the time and frequency response & stability analysis of digital control systems.

(iv) Identify the desired control specifications and will be able to design control algorithms

(v) Test & evaluate the design in simulation

UNIT I REVIEW OF CONTINUOUS CONTROL SYSTEM 9

Review of frequency and time response analysis and specifications of control systems, need for controllers, continoues time compensations, continoues time PI, PD, PID controllers, digital PID controllers.

UNIT II SIGNAL PROCESSING IN DIGITAL CONTROL 9

Sampling, time and frequency domain description, aliasing, hold operation, mathematical model of sample and hold, zero and first order hold, factors limiting the choice of sampling rate, reconstruction.

UNIT III MODELING AND ANALYSIS OF SAMPLED DATA CONTROL SYSTEM 9

Difference equation description, Z-transform method of description, pulse transfer function, time and frequency response of discrete time control systems, stability of digital control systems, Jury's stability test, state variable concepts, first companion, second companion, Jordan canonical models, discrete state variable models, elementary principles.

UNIT IV DESIGN OF DIGITAL CONTROL ALGORITHMS 9

Review of principle of compensator design, Z-plane specifications, digital compensator design using frequency response plots, discrete integrator, discrete differentiator, development of digital PID controller, transfer function, design in the Z-plane.

UNIT V PRACTICAL ASPECTS OF DIGITAL CONTROL ALGORITHMS 9

Algorithm development of PID control algorithms, software implementation, implementation using microprocessors and microcontrollers, finite word length effects, choice of data acquisition systems, microcontroller based temperature control systems, microcontroller based motor speed control systems.

L=45 T=15 Total=60

REFERENCES

1. M.Gopal, "Digital Control and Static Variable Methods", Tata McGraw Hill, New Delhi, 1997.
2. John J. D'Azzo, "Constantive Houpios, Linear Control System Analysis and Design", Mc Graw Hill, 1995.
3. Kenneth J. Ayala, "The 8051 Microcontroller- Architecture, Programming and Applications", Penram International, 2nd Edition, 1996.

PAL204 HIGH PERFORMANCE COMMUNICATION NETWORKS

L	T	P	C
3	1	0	4

Goal

To get an insight into the concepts of high performance communication networks such as packet switched system, ISDN, ATM and advanced networking.

Objectives

The course should enable the students to:

(i) Study the basics of Packet Switched Networks.

(ii) Study about the overview of ISDN and BROADBAND ISDN and the standards of digital end-to-end circuit switched services,

(iii) Study the ATM(Asynchronous Transfer Mode) and Frame Relay

(iv) Study the Advanced Network Architecture in connection with the Communication of Digital signals

(v) Study about the Blue Tooth Technology.

Outcome

At the end of the course the student should be able to:

(i) know about the digital communications network that groups all transmitted data, irrespective of content, type, or structure into suitably sized blocks with the IEEE stabndards.

(ii) know the communication standards for simultaneous digital transmission of voice, video, data, and other network services over the traditional circuits of the public switched telephone network.,

(iii) Understand wide area network technology and the telecommunications concept defined by ANSI and ITU standards for carriage of a complete range of user traffic, including voice, data, and video signals.

(iv) Know the IP forwarding architectures overlay model, Multi Protocol Label Switching integrated services in the Internet and related protocols.

(v) Understand the wireless technology for exchanging data over short distance and various protocols associated with the transmission.

UNIT I PACKET SWITCHED NETWORKS 9

OSI and IP models, Ethernet (IEEE 802.3), Token ring (IEEE 802.5), Wireless LAN (IEEE 802.11) FDDI, DQDB, SMDS: Internetworking with SMDS

UNIT II ISDN AND BROADBAND ISDN 9

ISDN - overview, interfaces and functions, Layers and services - Signaling System 7 - Broadband ISDN architecture and Protocols.

UNIT III ATM AND FRAME RELAY 9

ATM: Main features-addressing, signaling and routing, ATM header structure-adaptation layer,management and control, ATM switching and transmission.Frame Relay: Protocols and services, Congestion control, Internetworking with ATM, Internet and ATM, Frame relay via ATM.

UNIT IV ADVANCED NETWORK ARCHITECTURE 9

IP forwarding architectures overlay model, Multi Protocol Label Switching (MPLS), integrated services in the Internet, Resource Reservation Protocol (RSVP), Differentiated services

UNIT V BLUE TOOTH TECHNOLOGY 9

The Blue tooth module-Protocol stack Part I: Antennas, Radio interface, Base band, The Link controller, Audio, The Link Manager, The Host controller interface; The Blue tooth module-Protocol stack Part I: Logical link control and adaptation protocol, RFCOMM, Service discovery protocol,Wireless access protocol, Telephony control protocol.

L=45 ,T=15,Total=60

REFERENCE BOOKS :

1. William Stallings,"ISDN and Broadband ISDN with Frame Relay and ATM", 4th edition, Pearson education Asia, 2002.
2. Leon Gracia, Widjaja, "Communication networks ", Tata McGraw-Hill, New Delhi, 2000.
3. Jennifer Bray and Charles F.Sturman,"Blue Tooth" Pearson education Asia, 2001.
4. Sumit Kasera, Pankaj Sethi, "ATM Networks ", Tata McGraw-Hill, New Delhi, 2000.

5. Rainer Handel, Manfred N.Huber, Stefan Schroder,"ATM Networks",3rd edition, Pearson education asia,2002.

6. Jean Walrand and Pravin varaiya, "High Performance Communication networks", 2nd edition, Harcourt and Morgan Kauffman, London 2000.

7. William Stallings,"High-speed Networks and Internets", 2nd edition, Pearson education Asia, 2003.

PAL205 ELECTRONICS DESIGN LABORATORY II

L	T	P	C
0	0	3	2

Goal

To give hands on experience about PLL,CPLD/FPGA, embedded, micro controller and MATLAB simulation.

Objectives

The course will enable the students to:

(i) Know the design of PLL and a application

(ii) Know the modeling of Sequential digital systems using VHDL & verilog.

(iii) Implement applications using FPGA/CPLD.

(iv) Understand Simulations using MATLAB

(v) Understand Microcontroller Applications

Outcome

At the end of the course the students should be able to

(i) Design PLL and application involved PLL.

(ii) Design sequential circuits using VHDL and Verilog HDL.

(iii) Do implementations in FPGA/CPLD.

(iv) Do Simulations using MATLAB.

(v) Run applications in the given Microcontroller.

List of Experiments:

1. System design using PLL
2. System design using CPLD/FPGA
3. Alarm clock using embedded micro controller
4. Model train controller using embedded micro controller
5. Elevator controller using embedded micro controller

6. Simulation of Non adaptive Digital Control System using MAT LAB control system toolbox

7. Simulation of Adaptive Digital Control System using MAT LAB control system toolbox

Total = 45

ELECTIVE COURSES
PAL701 NEURAL NETWORKS AND APPLICATIONS

L	T	P	C
3	1	0	4

Goal

To impart knowledge on different neural networks and applications.

Objectives

The course should enable the students to:

(i) impart knowledge on the basics of neural networks and learning algorithms.

(ii) learn more about pattern recognition XOR, Problem and support vector machine.

(iii) impart knowledge on different models their learning strategies.

(iv) learn about associative learning adaptive resonance and memory models for implementation.

(v) impart knowledge about spiking neural model self organizing map.

Outcome

At the end of the course the student should be able to:

(i) select different neural network models and learning according to the application

(ii) select the support vector machines.

(iii) compare select different models for different application and their learning methods.

(iv) explain in detail about error correction in BAMS and adaptive BAMS.

(v) explain what is self organizing maps

UNIT I BASIC LEARNING ALGORITHM 9

Biological Neuron - Artificial Neural Model - Types of activation functions - Architecture: Feedforward and Feedback - Learning Process: Error Correction Learning -Memory Based Learning - Hebbian Learning - Competitive Learning - Boltzman Learning - Supervised and Unsupervised Learning - Learning Tasks: Pattern Space - Weight Space - Pattern Association - Pattern Recognition - Function Approximation - Control - Filtering - Beamforming - Memory - Adaptation - Statistical Learning Theory - Single Layer Perceptron - Perceptron Learning Algorithm - Perceptron Convergence Theorem - Least Mean Square Learning Algorithm - Multilayer Perceptron - Back Propagation Algorithm - XOR problem - Limitations of Back Propagation Algorithm.

UNIT II RADIAL-BASIS FUNCTION NETWORKS AND SUPPORT VECTOR MACHINES 9

Cover's Theorem on the Separability of Patterns - Exact Interpolator - Regularization Theory -

Generalized Radial Basis Function Networks - Learning in Radial Basis Function Networks - Applications: XOR Problem - Image Classification.

Optimal Hyperplane for Linearly Separable Patterns and Nonseparable Patterns - Support Vector Machine for Pattern Recognition - XOR Problem - -insensitive Loss Function - Support Vector Machines for Nonlinear Regression

UNIT III COMMITTEE MACHINES AND NEURODYNAMICS SYSTEMS 9

Ensemble Averaging - Boosting - Associative Gaussian Mixture Model - Hierarchical Mixture of Experts Model(HME) - Model Selection using a Standard Decision Tree - A Priori and Postpriori Probabilities - Maximum Likelihood Estimation - Learning Strategies for the HME Model - EM Algorithm - Applications of EM Algorithm to HME Model

Dynamical Systems - Attractors and Stability - Non-linear Dynamical Systems- Lyapunov Stability - Neurodynamical Systems - The Cohen-Grossberg Theorem.

UNIT IV ATTRACTOR NEURAL NETWORKS AND ADAPTIVE RESONANCE THEORY 9

Associative Learning - Attractor Neural Network Associative Memory - Linear Associative Memory - Hopfield Network - Content Addressable Memory - Strange Attractors and Chaos - Error Performance of Hopfield Networks - Applications of Hopfield Networks - Simulated Annealing - Boltzmann Machine - Bidirectional Associative Memory - BAM Stability Analysis - Error Correction in BAMs - Memory Annihilation of Structured Maps in BAMS - Continuous BAMs - Adaptive BAMs - Applications

Noise-Saturation Dilemma - Solving Noise-Saturation Dilemma - Recurrent On-center -Off-surround Networks - Building Blocks of Adaptive Resonance - Substrate of Resonance Structural Details of Resonance Model - Adaptive Resonance Theory - Applications

UNIT V SELF-ORGANISING MAPS AND PULSED NEURON MODELS 9

Self-organizing Map - Maximal Eigenvector Filtering - Sanger's Rule - Generalized Learning Law - Competitive Learning - Vector Quantization - Mexican Hat Networks - Self-organizing Feature Maps - Applications

Spiking Neuron Model - Integrate-and-Fire Neurons - Conductance Based Models - Computing with Spiking Neurons.

L=45 T=15 Total=60

REFERENCES:

1. Satish Kumar, "Neural Networks: A Classroom Approach", Tata McGraw-Hill Publishing Company Limited, New Delhi, 2004.
2. Simon Haykin, "Neural Networks: A Comprehensive Foundation", 2ed., Addison Wesley Longman (Singapore) Private Limited, Delhi, 2001.
3. Martin T.Hagan, Howard B. Demuth, and Mark Beale, "Neural Network Design", Thomson Learning, New Delhi, 2003.
4. James A. Freeman and David M. Skapura, "Neural Networks Algorithms, Applications, and Programming Techniques, Pearson Education (Singapore) Private Limited, Delhi, 2003.

PAL702 ROBOTICS

L	T	P	C
3	1	0	4

Goal

To study the principles of robotics including kinematics, artificial intelligence and sensors used.

Objectives

The course will enable the students to:

(i) Know about Kinematics, Transformation Matrix etc

(ii) Understanding the computer vision techniques

(iii) Know about sensors and sensing devices

(iv) Know algorithms of AI for Robotics

(v) Integrate the concepts together to build ROBOTS

Outcome

At the end of the course the students should be able to

(i) Solve problems involved in transformation matrices and the other concepts learned and to use them for building Robots.

(ii) Explain the computer vision techniques and use them for robotics.

(iii) Use the knowledge of sensors and sensing devices for Robots.

(iv) Explain the algorithms of AI and to use the same for building Robots.

(v) Explain how to build the ROBOTs by using concepts learned.

UNIT I INTRODUCTION TO ROBOTICS **9**

Motion - Potential Function, Road maps, Cell decomposition and Sensor and sensor planning. Kinematics. Forward and Inverse Kinematics - Transformation matrix and DH transformation. Inverse Kinematics - Geometric methods and Algebraic methods. Non-Holonomic constraints.

UNIT II COMPUTER VISION **9**

Projection - Optics, Projection on the Image Plane and Radiometry. Image Processing - Connectivity, Images-Gray Scale and Binary Images, Blob Filling, Thresholding, Histogram. Convolution - Digital Convolution and Filtering and Masking Techniques. Edge Detection - Mono and Stereo Vision.

UNIT III SENSORS AND SENSING DEVICES **9**

Introduction to various types of sensor. Resistive sensors. Range sensors - Ladar (laser distance and ranging), Sonar, Radar and Infra-red. Introduction to sensing - Light sensing, Heat sensing, Touch sensing and Position sensing.

UNIT IV ARTIFICIAL INTELLIGENCE **9**

Uniform Search strategies - Breadth first, Depth first, Depth limited, Iterative and deepening depth

first search and Bidirectional search. The A* algorithm . Planning - State-Space Planning , Plan-Space Planning, Graphplan/SatPlan and their Comparison, Multi-agent planning 1, and Multi-agent planning 2, Probabilistic Reasoning - Bayesian Networks, Decision Trees and Bayes net inference.

UNIT V INTEGRATION TO ROBOT **9**

Building of 4 axis or 6 axis robot - Vision System for pattern detection - Sensors for obstacle detection - AI algorithms for path finding and decision making

L=45 T=15 Total= 60

REFERENCES

1. Duda, Hart and Stork, Pattern Recognition. Wiley-Interscience, 2000.
2. Mallot, Computational Vision: Information Processing in Perception and Visual Behavior. Cambridge, MA: MIT Press, 2000.
3. Artificial Intelligence-A Modern Approach By Stuart Russell and Peter Norvig, Pearson Education Series in Artificial Intelligence, 2004
4. Fundamentals of Robotics, Analysis and control By Robert Schilling and Craig, Hall of India Private Limied, New Delhi, 2003.
5. Computer Vision, A modern Approach By Forsyth and Ponce, Person Education, 2003.

PAL703 ASIC DESIGN

L	T	P	C
3	1	0	4

Goal

To introduce various techniques of synthesis, simulation and testing of ASIC.available in it.

Objectives

The course will enable the students to:

(i) Understand the ASICS types, CMOS logic and ASIC library design.

(ii) Programable ASICs and its Logic cells and I/O cells.

(iii) Programable ASICs Interconnect and Software

(iv) Logic synthesis, Simulation and testing

(v) ASIC construction, floor planning , Placement and Routing

Outcome

After completion of the course the students are expected to be able to:

(i) Explain types of ASICs, technology involved for sequential,combinational and datapath logic cells

(ii) Explain Programmable ASICs and its Logic cells and I/O cells of different vendors.

(iii) Explain ASICs Interconnect and software

(iv) Explain Logic Synthesis, Simulation and testing.

(v) Explain ASIC construction, floor planning, placement and routing

UNIT I INTRODUCTION TO ASICS, CMOS LOGIC AND ASIC LIBRARY DESIGN 9

Types of ASICs - Design flow - CMOS transistors CMOS Design rules - Combinational Logic Cell - Sequential logic cell - Data path logic cell - Transistors as Resistors - Transistor Parasitic Capacitance- Logical effort -Library cell design - Library architecture .

UNIT II PROGRAMMABLE ASICS, PROGRAMMABLE ASIC LOGIC CELLS AND PROGRAMMABLE ASIC I/O CELLS 9

Anti fuse - static RAM - EPROM and EEPROM technology - PREP benchmarks - Actel ACT - Xilinx LCA -Altera FLEX - Altera MAX DC & AC inputs and outputs - Clock & Power inputs - Xilinx I/O blocks.

UNIT III PROGRAMMABLE ASIC INTERCONNECT, PROGRAMMABLE ASIC DESIGN SOFTWARE AND LOW LEVEL DESIGN ENTRY 9

Actel ACT -Xilinx LCA - Xilinx EPLD - Altera MAX 5000 and 7000 - Altera MAX 9000 - Altera FLEX - Design systems - Logic Synthesis - Half gate ASIC -Schematic entry - Low level design language - PLA tools -EDIF- CFI design representation.

UNIT IV LOGIC SYNTHESIS, SIMULATION AND TESTING 9

Verilog and logic synthesis -VHDL and logic synthesis - types of simulation -boundary scan test - fault simulation - automatic test pattern generation.

UNIT V ASIC CONSTRUCTION, FLOOR PLANNING, PLACEMENT AND ROUTING 9

System partition - FPGA partitioning - partitioning methods - floor planning - placement - physical design flow -global routing - detailed routing - special routing - circuit extraction - DRC.

L=45 T=15 Total=60

REFERENCES

1. M.J.S .Smith, "Application Specific Integrated Circuits, Addison -Wesley Longman Inc., 1997.
2. Farzad Nekoogar and Faranak Nekoogar, From ASICs to SOCs: A Practical Approach, Prentice Hall PTR, 2003.
3. Wayne Wolf, FPGA-Based System Design, Prentice Hall PTR, 2004.
4. R. Rajsuman, System-on-a-Chip Design and Test. Santa Clara, CA: Artech House Publishers, 2000.
5. F. Nekoogar. Timing Verification of Application-Specific Integrated Circuits (ASICs). Prentice Hall PTR, 1999.

PCS708 ELECTROMAGNETIC INTERFERENCE AND COMPATIBILITY IN SYSTEM DESIGN
Common to MTECH (CS)/M.TECH(EC)

L	T	P	C
3	1	0	4

Goal

To study source of EMI, standards, testing equipments and compatibility measures for equipments and PCBs.

Objectives

The course will enable the students to:

(i) understand the Electromagnetic interference concepts and its environment

(ii) understand the different kinds of EMI coupling.

(iii) know the EMI/EMC standards and to know the various measurement arrangements and methods.

(iv) know different types EMI control techniques .

(v) understand the Electro Magnetic Compatibility design for PCB's

Outcome

After completion of the course, the students are expected to:

(i) Gain sound knowledge about EMI concepts and its environment .

(ii) have knowledge in different kinds of EMI Coupling

(iii) gain sound knowledge in EMI/EMC standards , various measurement arrangements and techniques

(iv) have knowledge in EMI controlling techniques.

(v) Learn the concepts of EMC and to design PCB's with the inherent EMC.

UNIT I EMI ENVIRONMENT **9**

EMI/EMC concepts and definitions, Sources of EMI, conducted and radiated EMI, Transient EMI, Time domain Vs Frequency domain EMI, Units of measurement parameters, Emission and immunity concepts, ESD.

UNIT II EMI COUPLING PRINCIPLE **9**

Conducted, Radiated and Transient Coupling, Common Impedance Ground Coupling, Radiated Common Mode and Ground Loop Coupling, Radiated Differential Mode Coupling, Near Field Cable to Cable Coupling, Power Mains and Power Supply coupling.

UNIT III EMI/EMC STANDARDS AND MEASUREMENTS **9**

Civilian standards - FCC,CISPR,IEC,EN,Military standards - MIL STD 461D/462, EMI Test Instruments /Systems, EMI Shielded Chamber, Open Area Test Site, TEM Cell, Sensors/Injectors/Couplers, Test beds for ESD and EFT, Military Test Method and Procedures (462).

UNIT IV EMI CONTROL TECHNIQUES **9**

Shielding, Filtering, Grounding, Bonding, Isolation Transformer, Transient Suppressors, Cable Routing, Signal Control, Component Selection and Mounting.

UNIT V EMC DESIGN OF PCBs **9**

PCB Traces Cross Talk, Impedance Control, Power Distribution Decoupling, Zoning, Motherboard Designs and Propagation Delay Performance Models.

L=45 T=15 Total =60

REFERENCES

1. Henry W.Ott, "Noise Reduction Techniques in Electronic Systems", John Wiley and Sons, NewYork. 1988.
2. C.R.Paul, "Introduction to Electromagnetic Compatibility" , John Wiley and Sons, Inc, 1992
3. V.P.Kodali, "Engineering EMC Principles, Measurements and Technologies", IEEE Press, 1996.
4. Bernhard Keiser, "Principles of Electromagnetic Compatibility", Artech house, 3rd Ed, 1986.

PVL703 LOW POWER VLSI DESIGN

L	T	P	C
3	1	0	4

Goal

To understand the basics and advanced techniques in low power design, reduction in power dissipation, reduction in size, cost and etc.

Objectives

The course should enable the students to

1. Learn the design of low power ICS
2. Learn the Power Dissipation mechanism in various devices,
3. Learn the Design and test for Low power devices and optimization techniques involved in the design,
4. Learn the design and test for low power memory devices,
5. Learn the Software design for low power devices.

Outcomes

At the end of the course the student should be able to:

1. Understand the sources of power dissipation, power dissipation in MOSFET devices,
2. Understand the calculation for signal activity estimation and estimation of power in circuit level,

3. Understand the logic level and circuit optimization for low power circuits. Also to understand the design and testing of low power CMOS circuits,

4. Understand the low power static RAM Architectures, designing and testing of memory devices with low power dissipation,

5. Understand the sources of software power dissipation, software power estimation and its design.

UNIT I DESIGN OF LOW POWER ICs 9

Introduction - Sources of power dissipation - Design for low power - Power dissipation in MOSFET devices - Power dissipation in CMOS -Low power design limits

UNIT II PROBABILITY CALCULATION AND ESTIMATION OF POWER IN CIRCUIT LEVEL 9

Signal probability calculation-Probabilistic calculation for signal activity estimation-Statistical techniques for estimating average power in combinational and sequential circuits-Estimation of glitching power -Sensitivity analysis-Estimation of power in circuit level and IT based approaches.

UNIT III DESIGN AND TEST FOR LOW POWER CMOS CIRCUITS 9

Synthesis for low power - Behavioral level transforms-Logic level optimization for low power circuit level optimization and transforms-Future directions-design and test of low power CMOS circuits-Circuit design style-Leakage current in deep sub micrometer device design issues-low voltage design techniques.

UNIT IV SYNTHESIS FOR LOW POWER & TEST OF LOW VOLTAGE CMOS CIRCUITS 9

Low power static RAM architectures- MOS static RAM memory cell -Organization of SRAMs-Reducing voltage swing, power - Low energy computing-Energy dissipation in transistor channels-Energy recovery circuit design - Design with partially reversible logic-Supply clock generation.

UNIT V SOFTWARE DESIGN FOR LOW POWER 9

Software design for low power - Sources of software power dissipation - Software power estimation - Software power optimization - Automated low power code generation - Co design for low power.

L = 45, T = 15 TOTAL = 60

TEXT BOOK:

1. Kaushik Roy , Sharat C. Prasad "Low power CMOS VLSI circuit design" "A Wiley Inter science Publications". (1987)

REFERENCE:

1. Gary Yeap "Practical Low Power Digital VLSI Design", 1997

PAL704 DIGITAL SIGNAL PROCESSORS
Common to MTECH (PED)

L	T	P	C
3	1	0	4

Goal

To familiarize the students with modern digital processing techniques with emphasis on special processors for motor control.

Objectives

The course will enable the students to:

(i) understand about the architecture and algorithms of DSPs.Algorithms for signal processing-Basic architecture of DSPs

(ii) understand the students about the architecture, addressing modes, instruction set, programming.

(iii) know the students different I/O devices for DSPs for different Applications.Peripherals- Memory-Applications.

(iv) study the D to A interface and DMA, Serial Ports.

(v) familiarize the students about special processors available for motor control.

Outcome

After completion of the course the students are expected to be able to:

(i) get clear idea about the basic structure of DSPs.

(ii) write programming in Texas Processors once they understand the instruction set.

(iii) know the students different I/O devices for DSPs for different Applications.Peripherals- Memory-Applications

(iv) get a great exposure to interface different external I/O devices with processor.

(v) implement different control techniques of special purpose DSPs for various applications.

UNIT I INTRODUCTION **9**

Algorithms for signal processing - Basic architecture of DSPs.

UNIT II TEXAS PROCESSORS **9**

Architecture - Addressing modes - Instruction set - Programming

UNIT III PERIPHERALS INTERFACES OF DSP **9**

Peripherals - memory - Applications.

UNIT IV EXTERNAL INTERFACE **9**

Digital and analog Interface - Host interface - Memory interface - DMA ports - Serial ports.

UNIT V SPECIAL PROCESSORS FOR MOTOR CONTROL **9**

Architecture - Special features - PWM generation - controller implementation

L = 45 T = 15 TOTAL = 60

REFERENCES

1. K.Padmanabhan et al. "A Practical approach to Digital Signal Processing", New Age Publications, 2001.
2. B. Venkataramani et al. "Digital Signal Processor - Architecture, Programming and Applications", TMH, New Delhi 2002.
3. Texas Instruments - Manuals.

PCS706 DIGITAL IMAGE PROCESSING
Common to M.TECH(ES)

L	T	P	C
3	1	0	4

Goal

To introduce the students to various image processing techniques.

Objectives

The course should enable the students to:

(i) Study the image fundamentals,

(ii) Study the mathematical transforms necessary for image processing,

(iii) Study the image enhancement techniques and image estoration procedures,

(iv) Study the image segmentation and recognition techniques,

(v) Study the various image compression methods,

Outcome

At the end of the course the student should be able to:

(i) Understand the image fundamentals,

(ii) Understand the two dimensional image transforms,

(iii) Understand how to improve the image quality by using enhancement techniques and Restore the image by the use of various filtering techniques,

(iv) Understand the various segmentation methods and recognition techniques,

(v) Understand the various image compression techniques.

UNIT I DIGITAL IMAGE FUNDAMENTALS **12**

Elements of digital image processing systems, Elements of visual perception, psycho visual model, brightness, contrast, hue, saturation, mach band effect, Color image fundamentals -RGB,HIS models, Image sampling, Quantization, dither, Two-dimensional mathematical preliminaries.

UNIT II IMAGE TRANSFORMS **12**

1D DFT, 2D transforms - DFT, DCT, Discrete Sine, Walsh, Hadamard, Slant, Haar, KLT, SVD, Wavelet Transform.

UNIT III IMAGE ENHANCEMENT AND RESTORATION **12**

Histogram modification and specification techniques, Noise distributions, Spatial averaging, Directional Smoothing, Median, Geometric mean, Harmonic mean, Contraharmonic and Yp mean filters, Homomorphic filtering, Color image enhancement. Image Restoration - degradation model, Unconstrained and Constrained restoration, Inverse filtering - removal of blur caused by uniform linear motion, Wiener filtering, Geometric transformations - spatial transformations, Gray-Level interpolation.

UNIT IV IMAGE SEGMENTATION AND RECOGNITION **12**

Edge detection. Image segmentation by region growing, region splitting and merging, edge linking.. Image Recognition - Patterns and pattern classes, Matching by minimum distance classifier, Matching by correlation, Back Propagation Neural Network, Neural Network applications in Image Processing.

UNIT V IMAGE COMPRESSION **12**

Need for data compression, Huffman - Run Length Encoding, Shift codes, Arithmetic coding, Vector Quantization, Block Truncation Coding. Transform Coding - DCT and Wavelet - JPEG - MPEG. Standards, Concepts of Context based Compression.

L = 45, T = 15, TOTAL= 60

TEXT BOOKS

1. Rafael C. Gonzalez, Richard E.Woods, 'Digital Image Processing', Pearson Education, Inc., Second Edition, 2007.
2. Anil K. Jain, 'Fundamentals of Digital Image Processing', Prentice Hall of India, 2002.

REFERENCES:

1. David Salomon : Data Compression - The Complete Reference, Springer Verlag New York Inc., 2nd Edition, 2001
2. Rafael C. Gonzalez, Richard E.Woods, Steven Eddins, ' Digital Image Processing using MATLAB', Pearson Education, Inc., 2004.
3. William K.Pratt, ' Digital Image Processing', John Wiley, NewYork, 2002.
4. Milman Sonka, Vaclav Hlavac, Roger Boyle, 'Image Processing, Analysis, and Machine Vision', Brooks/Cole, Vikas Publishing House, II ed., 1999.
5. Sid Ahmed, M.A., 'Image Processing Theory, Algorithms and Architectures', McGrawHill, 1995.