RESOURCE PERSONS

Mr. G. Prakash
Lead Application Engineer,
CoreEL Technologies, Bangalore.

Mr. V. Senthilmurugan
Manager - University Relations,
CoreEL Technologies, Bangalore.
Mobile Number : +91-7708233133

REGISTRATION DETAILS

Faculty/Corporate Members : Rs.1500
Research Scholars/ UG/PG Students : Rs.1200

Registration fee should to be drawn in favor of "Hindustan Institute of Technology and Science" payable at Chennai. Fill in the form and send the scan copy of both the application and DD to the mail id mentioned below. The hard copy of the application and the DD is to be sent to the Coordinator on or before 11-07-2018. Selection will be on the First come and First Serve basis.

Important Dates

Receipt of Application	: 11-07-2018
Intimation of Selection	: 18-07-2018

Travel and Accommodation

No TA/DA will be provided. Paid Accommodation can be arranged on request

CHIEF PATRON
Dr. (Mrs.) Elizabeth Verghese, Chancellor
PATRONS
Dr. Anand Jacob Verghese, Pro Chancellor
Dr. K.P. Isaac, Vice Chancellor
CO-PATRONS
Mr. Ashok Verghese, Director
Dr. Aby Sam, Director
Dr. Pon Ramalingam, Registrar
Dr. N. Vasudevan, Dean – Academics
TECHNICAL ADVISORY COMMITTEE
Dr.G.Illavazhagan, Director – Research
Dr.Baby Joseph, Dean-Research
Dr.D.Mohan,Associate, Dean-Research
Dr.Aby.K.Thomas, Prof. & Head / ECE
CONVENORS
Mr. M.Rajmohan, Assistant Professor/ECE
Mr. D. Sahaya lenin, Assistant Professor/ECE
Mr. P. Ramesh, Assistant Professor/ECE

ADDRESS FOR CORRESPONDENCE

Mr. M. RAJMOHAN
Assistant Professor, Department of ECE
Hindustan Institute of Technology & Science
P.O. BoxNo. 1,Rajiv Gandhi Salai, Padur - 603103
Chennai, Tamilnadu
Contact No: 9789573075 / 9442703166
Email: mrajmohan@hindustanuniv.ac.in

HINDUSTAN
INSTITUTE OF TECHNOLOGY & SCIENCE
(DEEMED TO BE UNIVERSITY)

Two Days National
Workshop
on

SYSTEM DESIGN USING VIVADO SUITE AND ZYNQ-7000 SOC

July 23rd & 24th 2018

Organized by
DEPARTMENT OF ELECTRONICS AND COMMUNICATION ENGINEERING

Convenors
Mr. M.RAJMOHAN, Asst.prof. / ECE
Mr. D. SAHAYA LENIN, Asst.Prof / ECE
Mr. P. RAMESH, Asst.Prof / ECE

in association with
CoreEL Technologies Enabling Excellence | XILINX | DIGILENT

ABOUT THE INSTITUTION

Hindustan Institute of Technology & Science (HITS) is one of the leading institutions in India with an excellent and established academic and research standing. The main campus is located on the outskirts of Chennai, India. HITS conferred the "University Status" by the University Grant Commission (UGC), Government of India under the section 3 of the UGC act 1956. NAAC has accredited HITS with 'A' Grade. QS has Ranked HITS with QS 3 Star Ratings. HITS completed 31 years of dedicated service to the nation generating trained and qualified graduates for the country. The University has accomplished its mission and its academic achievements are a testimony to the same. It has students and faculty exchange programs with the leading international universities. The university has also received numerous awards over the years

ABOUT THE DEPARTMENT

Electronics and Communication Engineering at HITS has a long standing tradition of excellence. The Department has a team of well qualified experienced and dedicated faculty members with Industrial and Research background. The Department is fully equipped with state-of-the-art laboratories such as DSP, VLSI, Computer Networks, Digital, LIC and Microwave and FOC Laboratories and a (Ph.D) Research Centre

ABOUT COREEL TECHNOLOGIES

CoreEL Technologies (I) Pvt Ltd, CoreEL is a customer Application Specific Products & Solutions company offering Intellectual Property (IP) Hardware, Software & Engineering Services to customers, enabling them to Design Manufacture and Market world class electronic products. The portfolio of offerings include IP cores, System Design, Architecture, Validation, Sustenance, Prototype Manufacturing, Next-Gen products, Semiconductor solutions & Distribution of EDA Tools & COTS products. CoreEL was founded in 1999 and is an ISO 9001:2008 certified headquartered at Bangalore India

ABOUT COREEL UNIVERSITY PROGRAM

CoreEL University Program provides Eco-System support to Indian Academia in Engineering Higher Education, in the field of embedded systems thereby enabling the delivery of quality education. CoreEL university achieves this by providing state of the art products from XILINX, MENTOR GRAPHICS, MATLAB,ANSYS, VxWorks (WIND RIVER), Speedgoat (Rapid Controller Prototyping, Hardware-in-the-Loop simulation, and deployment,) PCB Design Tools from Mentor Graphics ,Analog Discovery Kits from Digilent (Analog Discovery kit can replace the conventional regulated power supply, Function Generator, Oscilloscope, and smaller parts like Bread board etc with one portable, compact and power effective and low cost solution!) to universities Multiyear application engineering support on these products Faculty and student training, providing industry specific inputs to update the curriculum and helping universities set up Centers of Excellence in Embedded Systems arena

PRE-REQUISITES

- Digital design experience
- Basic HDL knowledge (VHDL or Verilog)
- System level design experience using Xilinx FPGA
- Basic experience with Xilinx Vivado design software suite
- Good understanding of C programming

WORKSHOP AGENDA - DAY –1

- 7-Series Architecture Overview
- Vivado Design Flow
- Lab 1: Creating an HDL Design
- Use Vivado IDE to create a simple HDL design. Simulate the design using the XSIM HDL
- simulator available in Vivado design suite. Generate the bitstream and debug the design
- using Vivado Logic Analayzer
- IP Integrator and Embedded System Design Flow
- Lab 2: Create a Processor System using IP Integrator
- Create a simple ARM Cortex-A9 based processor design targeting the ZedBoard using IP
- Integrator.
- Lab 3: Debugging using Vivado Logic Analyzer cores
- Insert various Vivado Logic Analyzer cores to debug/ analyze system behavior.

DAY –2

- Embedded System Design with Custom IP
- Lab 4: Creating and Adding Your Own Custom IP
- Use the Manage IP feature of Vivado to create a custom IP and extend the system with the custom peripheral. Write a basic C application to access the peripherals.
- System Debugging using Vivado Logic Analyzer and SDK
- Lab 5: Debugging using Vivado Logic Analyzer cores
- Insert various Vivado Logic Analyzer cores to debug/ analyze system behavior.
- Profiling and Performance Improvement
- Introduction to High-Level Synthesis with Vivado HLS
- Improving Performance and Resource Utilization
- Creating an Accelerator
- Lab 6: Creating a Processor System using Accelerator
- Profile an application performing a function both in software and hardware. Create an accelerator in Vivado HLS. Use the generated accelerator to build a complete system.